# Process Development to Achieve a High Yield Wafer-to-Wafer (W2W) Hybrid Bond

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## ABSTRACT

Advanced wafer level packaging has been evolving with the need to scale down to sub-10um pitches due to limitations with current solder bumping techniques. Hybrid bonding technology facilitates the interconnection of tightly spaced metal pads in a 3D vertical stack configuration. The advantages of this packaging technique enable sub-10um pitch designs, increases the I/O density, expands device bandwidth, decreases power needs, improves device speed, etc. The focus of this paper is to discuss methodologies that ensure high yielding Cu-based wafer to wafer (W2W) hybrid bonding that include but not limited to description of the test vehicle used, chemical mechanical planarization, metrology, plasma activation, bonding techniques, annealing, CSAM feedback and cross sections to verify metal to metal pad diffusion.

Key words: Hybrid Bonding, chemical mechanical planarization [CMP], plasma activation, metrology, annealing, CSAM, W2W, 3D Vertical Stack, Advanced Packaging, atomic force microscopy [AFM], roughness, recess, rounding, flatness.

## INTRODUCTION

Wafer bonding are advanced semiconductor fabrication techniques enable the integration of different materials and structures at the wafer level. These techniques play a crucial role in the development of various electronic and photonic devices, such as microelectromechanical systems (MEMS), sensors, photonics, and advanced integrated circuits. This allows for the integration of dissimilar materials, which is essential for achieving desired functionalities in advanced devices. Wafer bonding can be classified into various types based on the bonding mechanisms and materials used with oxide and hybrid bonding being the two prominent approaches presented in this paper.

A) Oxide Wafer Bonding: Oxide wafer bonding, also known as direct bonding or fusion bonding, involves joining two silicon wafers together by exploiting the formation of strong silicon-oxygen (Si-O) bonds at the interface. At the high level the process typically involves the following steps:

- Surface Preparation: The surfaces of the wafers to be bonded are thoroughly cleaned to ensure a high-quality bond interface.
- Activation: The wafer surfaces go a thru a plasma process to prepare the surface to spontaneously bond with each other.
- Alignment: The wafers are either notch or precisely patterned aligned to achieve the desired orientation and alignment of the structures.
- Bonding: The wafers are brought into close contact under controlled conditions (e.g., force, pressure, temperature, etc.). At the interface, silicon atoms form covalent bonds with oxygen atoms, creating a strong and permanent bond.
- Annealing: The bonded wafers may undergo annealing to further increase the bond strength quality.

Oxide wafer bonding is widely used for applications where high bond strength, excellent thermal stability and hermetic sealing are required.

B) Hybrid Bonding: Hybrid wafer bonding involves joining two aligned wafers with an activated oxide layer to induce a van der waals attraction between the substrates to lock in place for the metal pads to thermally expand and diffuse to create metal-to-metal interconnections during the anneal process.

High level process involves the following steps:

- Surface Preparation: Like oxide bonding, the surfaces of the wafers are cleaned.
- Activation: The wafer surfaces go a thru a plasma process to prepare the surface to spontaneously bond with each other.
- Aligned Bonding: The wafers are aligned with patterned targets and brought into contact with the activated oxide layer spontaneously bonding together.
- Annealing: Thermal expansion and diffusion of the metal is achieved by annealing to create the metal-to-metal interconnects and improve bond strength.

Hybrid wafer bonding is advantageous for applications that require bonding various materials but is important to bond materials with similar coefficients of thermal expansion (CTE). It allows for the integration of materials with different thermal, optical, and electrical properties.

In summary, wafer bonding is an essential advanced packaging technique for integrating dissimilar materials and structures at the wafer level, enabling the development of advanced electronic and photonic devices with enhanced functionalities and performance. These techniques continue to drive innovation in semiconductor technology and contribute to the advancement of various industries.

## TEST VEHICLE

Development started on blank Prime Si wafers of standard thickness with an oxide thickness of 1500A that were chemically mechanically planarized (CMP) with metrology feedback from atomic force microscopy (AFM), profilometry and scanning acoustic microscopy (CSAM) post bonding. For the Hybrid Bond wafers a test vehicle was designed with 4um pads and an 8um pitch built around a 100um x 100um chip size. The design also incorporated a bond interconnect layer and a redistribution layer. Considerations for hybrid wafers consisted of the test vehicle layout and design, oxide layer, lithography, etch process, barrier layer, plating, CMP process, bonding process, and anneal conditions.

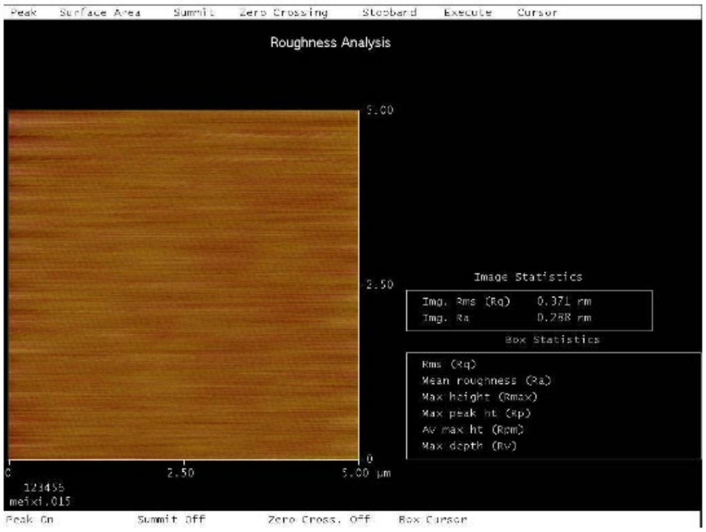
## PROCESS DEVELOPMENT APPROACH

There are several disciplines, techniques and processes that are required for viable wafer to wafer bonding (W2W) to be successful. These processes include but are not limited to silicon wafer orientation (bond strength), oxide type, lithography, barrier, plating, CMP, bow, cleaning, activation, bonding and anneal. The developments outlined in this paper is focused on the CMP and bonding processes that were developed for successful fusion and hybrid bonding.

## BONDING

Two different oxide bonding paths were run in parallel on 200mm blank standard prime Si wafers with thermal oxide that was grown with no further processing prior to bonding and deposited oxide that was chemically mechanically planarized (CMP) targeting a low surface roughness and flatness using AFM and profilometry for metrology feedback.

<u>CMP</u>**:** Surface roughness is one of the key metrics in achieving a strong covalent bond, see figure 1 [1] for an image using a Veeco Dimension 9000 (AFM). A low surface roughness is desired over a high surface roughness that will cause poor bonding due to larger irregularities across the wafer surface. The development process was first baselined by bonding a series of thermal oxide wafers that were not planarized and then by a series of oxide deposited wafers that were chemically mechanically planarized (CMP) with an AMAT Mirra. Several cycles of learning were run to find the best combination of slurry, pad type, head force, turntable speed and time for endpoint development for the process. To verify the CMP process output, post bond the wafers were analyzed using infrared microscopy and scanning acoustic microscopy (CSAM) to verify bond uniformity and for void detection within the bond interface, see figure 2. Surface planarity across the wafer is another key metric in achieving covalent bonding, this is controlled by an optimized CMP process and verified using a profilometer or AFM (shorter distances) to measure surface flatness across a set length, see figure 3.



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Img. Ra          0.288 nm
        Box Statistics
Rms (Rq)
Mean roughness (Ra)
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**Figure 1.** AFM image of Oxide surface roughness [1].

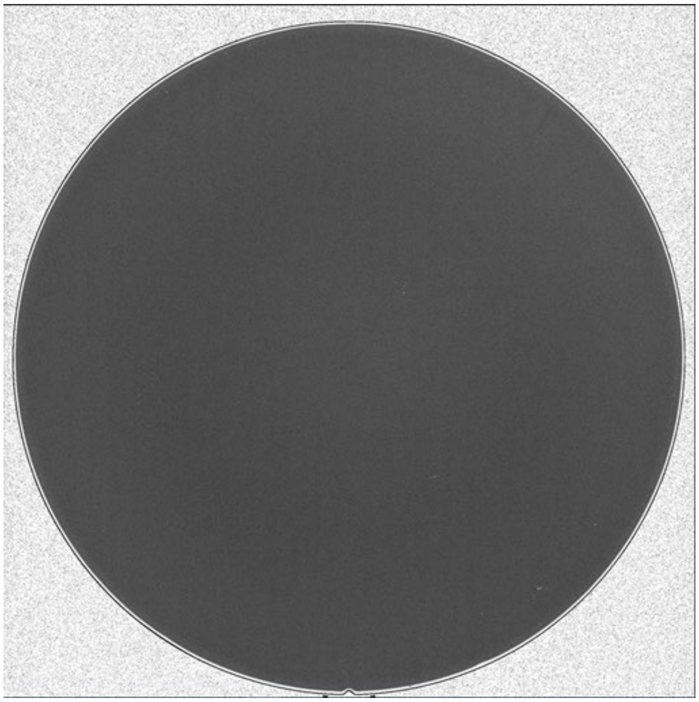


**Figure 2.** CSAM of Oxide Bond.

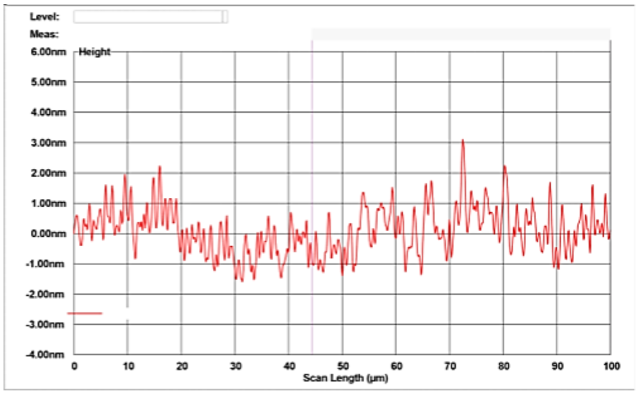


**Figure 3.** Flatness measurement thru profilometry.

The oxide bonding process developed was performed under atmosphere and ambient temperature using a SUSS XBS200 Wafer Bonder. The wafers were bonded by the methodology of center contact first and then slowly bringing the wafers together. Center contact first allows for air to be forced out evenly around the circumference of the wafer as the two interfaces come together. The wafer process flow incorporates cleaning, plasma, and hydration prior to performing the bond, see figure 4. Inspections are incorporated to review the quality of the bond prior to committing to anneal, in this scenario there's opportunity for rework and failure analysis.

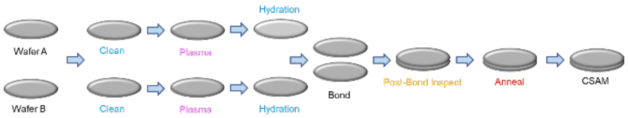
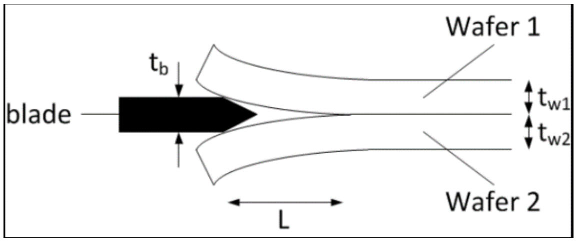


**Figure 4.** Bond Process Flow.

To meet the requirements of post wafer processing such as wafer grinding, bond strength which is shear resistance must be greater than 1.5 J/m² to survive back end of line (BEOL) processing.

Bond Strength: Shear resistance is part of wafer bond characterization and is accomplished thru a methodology called the Razor Blade test, also known as double cantilever beam test, see figure 5 [2].



$$\gamma = \frac{3t_b^2 E_1 t_{w1}^3 E_2 t_{w2}^3}{16L^4(E_1 t_{w1}^3 + E_2 t_{w2}^3)};$$

$t_b$ = Blade thickness
$t_w$ = Wafer Thickness
$E$ = young's modulus of Si
$L$ = Length of separation

**Figure 5.** Bond Strength Method & Equation.

Figure 6 shows the collected bond strength data between three different pairs of oxide deposited bonded wafers of that collectively exceed the minimum specification of 1.5 J / m², which is an industry standard value [3]. These wafers were measured in different time increments within a 60 second time frame under an Infrared Microscope observing the bond separation as a function of time.

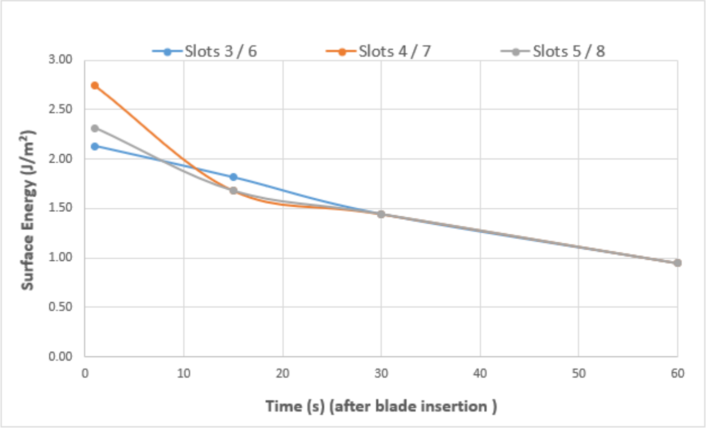


**Figure 6.** Bond Strength measured in (J / m²).

Achieving repeatable bond strength and oxide bond uniformity ensures both the CMP and bonding processes have been optimized to move on to Cu hybrid bonding development.

## HYBRID BONDING

The focus presented here will be on chemical mechanical planarization (CMP) and bonding techniques. A 4um pad 8um pitch test vehicle with a DBI and RDL layer was used to develop the Cu hybrid bonding process, see figure 7. The test vehicle also includes bonding alignment marks for overlay accuracy analysis of the bonding interface. Other processes equally important include but not limited to is the test vehicle layout and design, oxide layer, lithography, etch, plating and anneal.

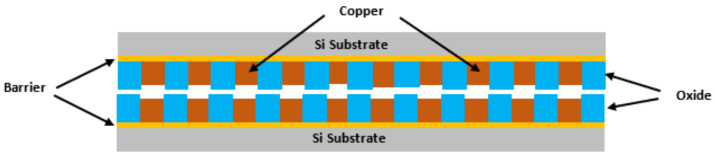


**Figure 7.** Test Vehicle with mating wafer.

CMP: After the test vehicle completes the Cu plating process, it goes into a designated Cu C.M.P process to remove the excess Cu and barrier layer from the surface to planarize and establish the proper surface roughness, Cu recess and oxide rounding as shown in a recent publication by Adeia, see figure 8 [3]. It is important to understand why proper Cu recess and oxide rounding are critical for successful hybrid bonding.

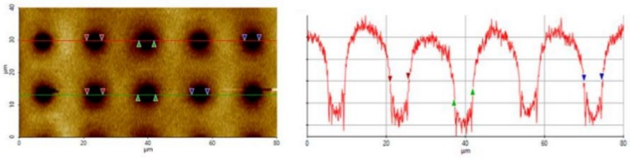


**Figure 8.** AFM profile after CMP [3].

Recess: Proper recess is necessary to allow the Cu to grow during the anneal process and fully diffuse with the mating wafer, see figure 9. If the recess is too shallow it will tend to push against the opposing Cu creating gaps on the bond interface and not uniformly diffusing, bond voids would be captured on CSAM.

With too much recess the Cu will plateau during thermal expansion and never fully realize diffusing into the mating metal pad. Unintentional micro-cavities will develop on the bond interface.

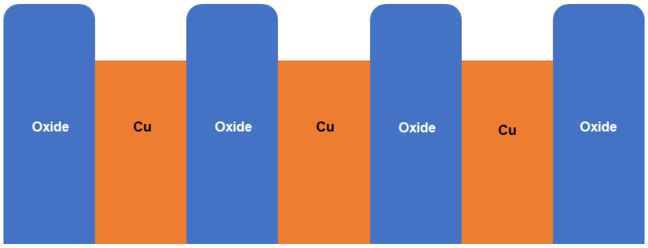


**Figure 9.** Cu recess (dishing) and oxide profile.

Rounding: Rounding determines how much of the planarized oxide surface contacts the mating wafer to achieve the initial covalent bond. If the oxide has a rounded profile, surface contact of the oxides of each wafer will be reduced weakening the bond strength, see figures 9 & 10.

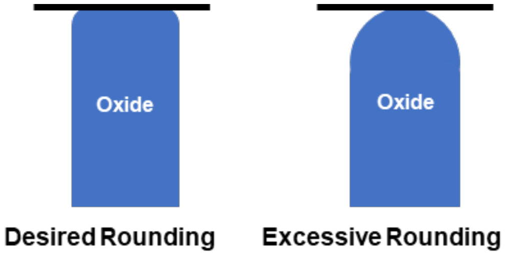


**Figure 10.** Contact profile Comparision.

Flatness: Profilometry is performed to verify the surface of the wafer is uniformly planarized. Flatness of the wafer surface improves the attraction of the two substrates by minimizing surface irregularities and topography that can inhibit strong bonds. Any nonuniformity present on the wafer will create challenges with non-uniform bonding and will appear as voids under CSAM, see figure 11. If the wafer is analyzed prior to anneal it is possible to rework the wafer, but new issues can arise with too much re-polishing of the surface.

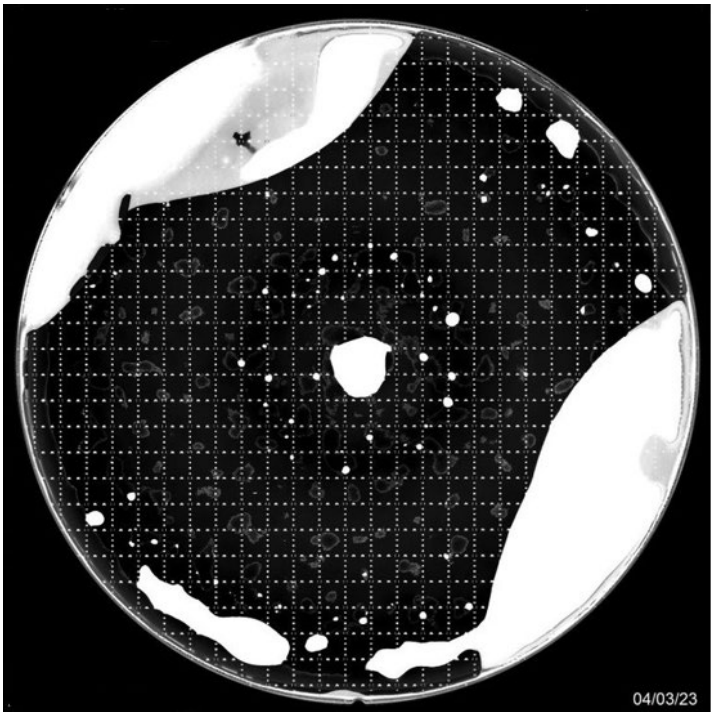


**Figure 11.** CSAM Image of voids due to uneven planarization.

Prior to bonding it's important to capture incoming wafer bow post CMP and run wafer surface particle scans to ensure incoming wafers meet bow and defect count targets.

Bow: The bow measurements were performed on a KLA Aset F5x Spectrometry tool, it's desired for wafer bow to be in a compressive state and not a tensile profile to ensure successful uniform bonding, see figure 12 [4]. Attempting to bond two wafers in a tensile profile will be challenging to make center contact uniformly and may induce small pockets of trapped air (bonding under atmosphere).

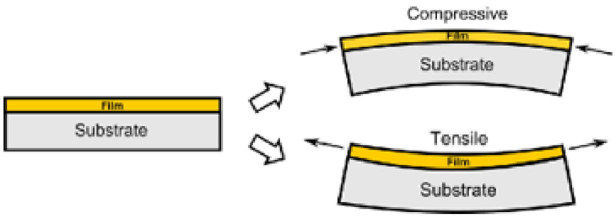


**Figure 12.** Stress Profiles [4].

Particles: Surface particles on the wafers were scanned using a KLA-Tencor 2139 Brightfield Patterned Surface Defect Inspection System for 200nm sized and larger defects. Wafer scans that exhibited surface contamination were run on an OnTrak DSS 200 Series 2 double-sided PVA scrubber and re-scanned to confirm the reduction of the surface particles. If wafers are bonded with high particle counts, it will lead to voids at the interface.

Bonding: The bonding process flow shares a lot of the same processing steps as fusion bonding as outlined in figure 4 using the SUSS XBS200 Wafer Bonder. The added step to hybrid bonding is training alignment marks into the vision software for high accuracy bonding to be achieved.

Wafer overlay measurements and infrared bond void detection can be run in situ within the SUSS XBS200 Wafer Bonder to determine if there's a rework opportunity based on the metrology feedback. Additionally, Scanning Acoustic Microscopy (CSAM) using a Nordson Sonoscan will provide an accurate wafer bond uniformity image before committing to annealing.

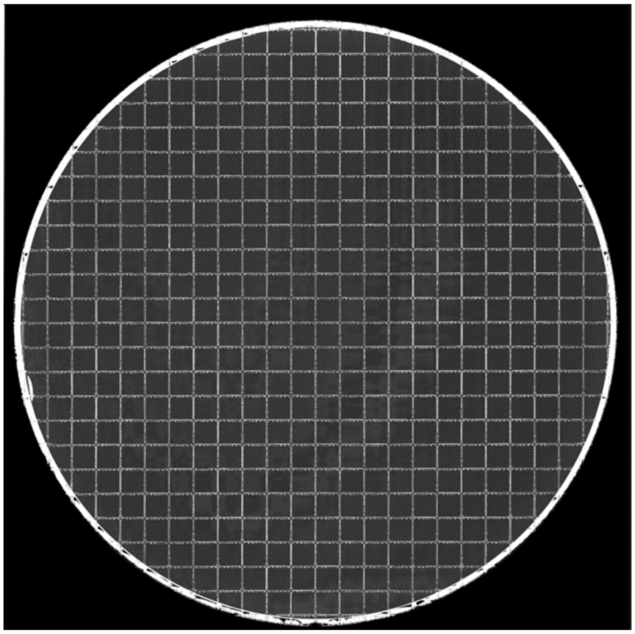


**Figure 13.** Hybrid Bonded Wafer CSAM Image.

## DISCUSSION

In this work, the development of a successful oxide W2W bond was first accomplished. Figure 6 shows all the oxide wafers evaluated for bond strength that exceeded the minimum bond strength target of 1.5 J/m$^2$ as a result from optimizing the surface roughness, flatness, plasma activation and bonding parameters. Wafer bow profile and cleanliness also contributed to successful bonding needing to be monitored. Upon achieving the ability to do successful oxide W2W bonding, further development in the CMP process was required for hybrid bonding to develop and optimize Cu recess and oxide rounding. Figure 13 shows a CSAM image of a successful W2W hybrid bond.

As previously mentioned under the test vehicle section, the bonding development was done a 200mm diameter wafer with a patterned layout consisting of a 4um pad on an 8um pitch. To successfully achieve a uniform Cu hybrid bond, all prior surface conditions discussed under the CMP sections must be achieved. This highlights why an optimized CMP process is critical in setting recess, rounding, and flatness for bonding to succeed. The bonding process must also have an optimized plasma activation process and bonding parameters for how the wafers come together. Annealing not discussed in detail here needs to be established to mitigate potential oxide out gassing and not to exceed the necessary temperature and time required for successful metal to metal diffusion.

## CONCLUSION

This effort has shown that both oxide and hybrid bonding can be successfully achieved using a 200mm wafer format once CMP and Bonding is optimized, and the appropriate metrology tools are available for this specific type of advanced packaging development.

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