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Low Temperature Solder Joint Shear Strength of Components in SMT Assembly

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ABSTRACT
Tin-Bismuth (Sn-Bi) Low Temperature Solder (LTS) pastes are being widely adopted by the electronics industry due to the benefits of lowering the peak reflow temperatures in SMT assembly. Lower peak temperatures result in reduced package and board warpage which leads to fewer assembly defects and higher yields. However, the effects of the paste metallurgy, especially the Bi content, on board level reliability are being actively researched. Temperature cycling and shock reliability performance evaluations have frequently been published. However, there is a lack of data assessing the shear strength of the LTS joints for actual motherboard components. Shear strength of the solder joints plays an important role in preventing damage due to board handling and such data is also useful for new solder paste development and evaluations.

Shear strength data was collected using a Mark-10 Test Frame on several SMT components that are prone to handling damage such as headers, inductors, crystal components, clips, shields, and PEM nuts. The influence of several assembly process parameters, such as reflow profiles and paste volumes, as well as incoming board properties such as pad surface finish have been studied in this work. Both LTS and Tin-Silver-Copper (SAC) paste metallurgies have been evaluated. This study was conducted on a test board designed specifically for performing shear testing and on actual product boards.

This paper shows that paste metallurgy has the most significant effect on the shear strength. Other process parameters such as reflow profiles have no impact on the shear strength if they are within the spec window provided by the paste supplier. This data will be helpful in bolstering the confidence of ODMs to move to LTS paste metallurgies for SMT assembly.

Key words: LTS, shear strength, assembly.

INTRODUCTION
Tin-Bismuth Low Temperature solder (LTS) refers to a class of solder alloys based on Sn-Bi with compositions typically containing 35-58% Bi. It has a melting point of close to 140ºC. Low temperature solder has been looked at by the industry as an alternative to the now prevalent Tin-Silver-Copper (SAC) solder to lower peak reflow temperatures during SMT from 250ºC to 190ºC, which can reduce the inherent board-to-package warpage by more than 50% [1,2]. This reduction in warpage proves to be significant as BGAs are shrinking in size and ball pitch is shrinking as well. If warpage is not controlled, ultrafine BGA yields will suffer [3]. LTS also helps with preventing damage to components in SMT assembly that cannot withstand high temperatures. Lower temperatures not only help in improving SMT yields of BGAs, but also allow for a more diverse set of components to be used thereby allowing more flexibility in board design and a reduction in overall costs. In addition, lower temperatures can help in avoiding adjacent component damage during rework. Low temperature solder also has an added benefit in reducing oven operational costs by running at lower temperatures thus using less electricity which aids in meeting green energy goals in the manufacturing sector.

One important criteria for driving acceptance of LTS pastes in the industry is the backward compatibility of LTS paste with BGAs having SAC balls. Such assembly is called mixed assembly or hybrid assembly as opposed to homogeneous joints. This allows factories to get the benefits of using the LTS paste without the need to alter the existing BOM of SMT components. However, there are several challenges with reliability and shock performance of hybrid joints. Since the commonly used LTS formulations are alloys based on a B-Sn binary phase diagram, inherent brittleness of bismuth results in poor mechanical shock resistance and fatigue resistance compared to SAC. Reducing the Bi content and microalloy additions can improve ductility [4-6].

Although there are several studies on the reliability and shock performance of LTS, these are primarily focused on the BGA joint reliability. There are very few studies on the performance of the non-BGA components on the board [7]. Shear strength of these joints is necessary of keep the components from falling off the board during handling. The components which are most prone to such damage are typically tall headers, E-Caps etc. As the ratio of the volume of the solder in the joint to the height of the component reduces, it become more prone to knock-off during handling.

This paper studies the effect of several factors on the shear strength of a wide range of components assembled using LTS paste. The study encompasses testing on real functional boards as well as a test board. Factors such as the effect of solder paste metallurgy, board surface finish, paste volume and reflow profile are measured.

EXPERIMENTAL METHOD

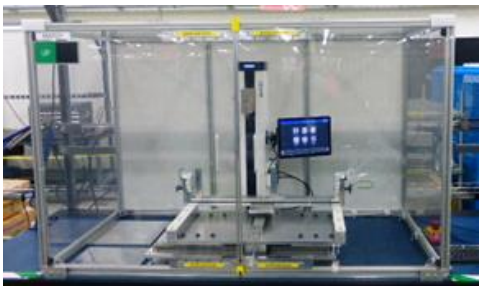
Shear testing was performed using a motorized force tester shown in Figure 1(a). A universal fixture was developed to grip boards with components on the top side to get consistent shear force values shown in Figure 1(b). All the shear testing was done at 300mm/s speed. Different tips were used to shear off the component depending on the size and location on the board. The force was plotted as function of time, as shown in Figure 1(c), and the max force in Kg-f was recorded.

Two functional boards were used for the study. The first board (Functional board #1) was a reference validation board that mimicked an ATX form factor motherboard that fit in a desktop computer with the dimensions of 280 x 230mm and 1.6mm thick. The second board (Functional board #2) was a laptop motherboard 161 x 45mm in size and 0.6mm thick. Both boards were densely populated with a variety of components. The solder pads were metal defined.

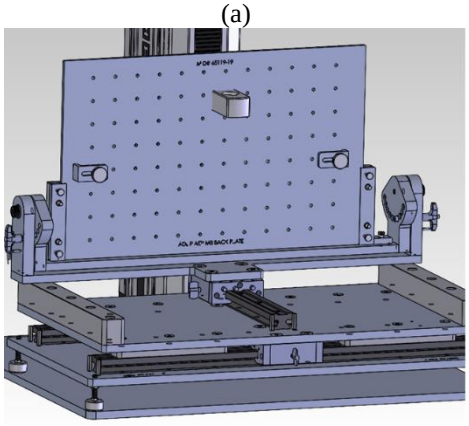
Two different types of functional boards shown in Figure 2(a) & (c) were assembled under different SMT conditions such as different stencil thickness, board surface finish and different solder paste. The details of the variations on these parameters are provided in Table 1. 3.81mm tall 3-pin headers marked as J11 in Figure 2(b) were sheared off these functional boards from different locations on the board. These tiny headers were chosen for testing since these are most prone to handling damage due to small pad area to support the tall header.

A 5" X 5" JEDEC shear test board shown in Figure 3 was also designed with OSP surface finish and Solder Mask Defined (SMD) pads. The PCB was 4 layers and 1mm thick. The board had 17 components including headers, shields, tall E-caps, crystals. They are listed in Table 2. These components are of interest because they are subjected to handling, plugging and unplugging. Torquing is also a risk due to size, height, and use conditions in the field or factory. The board covered various type of components with different termination styles and body sizes. The effect of a reflow profile on the max shear force was studied using this test board. The DOE legs as shown in Figure 4. There were four legs: three legs for LTS and one leg with a POR SAC profile. The formulation of the SAC paste was SAC305. The LTS paste used was a low temperature lead-free solder paste based on Sn-57Bi-X alloy which is a hypoeutectic alloy by adding element X to the traditional Sn42Bi58. The three LTS legs were designed to encompass the extremes of the paste supplier window: cold (low peak, low TAL), center (mid peak, mid TAL) and hot (high peak, high TAL). The LTS solder paste used was a eutectic paste. A 3 mil stencil was used for paste printing.

These functional and the JEDEC test boards were assembled in house at Intel. A widely used paste printing machine in the industry was used for printing the solder paste. Common Pick and Place tools were used for placement and an inline12 Zone heating Reflow oven was used to reflow the boards.



(a)



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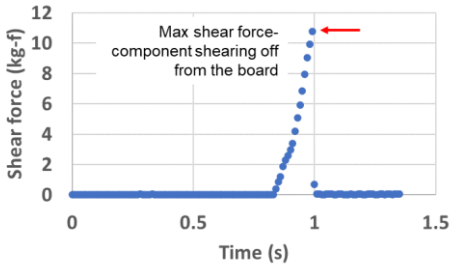
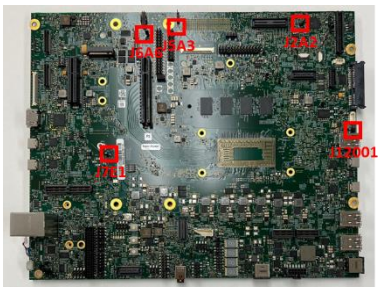
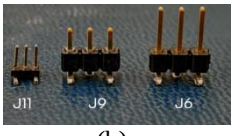


(c)

Figure 1. (a) Mark 10 F105-IMT shear test frame. (b) Universal fixture to hold boards with top side parts only. (c) Force curve for a typical shear test.



(a)



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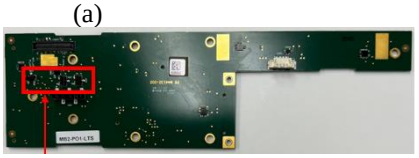


(c)

Figure 2. (a) Functional board#1 with locations of the 3-pin header. (b) 3-pin headers of various sizes J11 is 3.81 mm tall. (c) Functional board#2.

Table 1. Functional board testing details- Factors and variations

Solder Paste	Stencil Thickness	Board surface finish	Functional Board type
LTS	3mil	OSP	#1
SAC	4mil	ENIG	#2

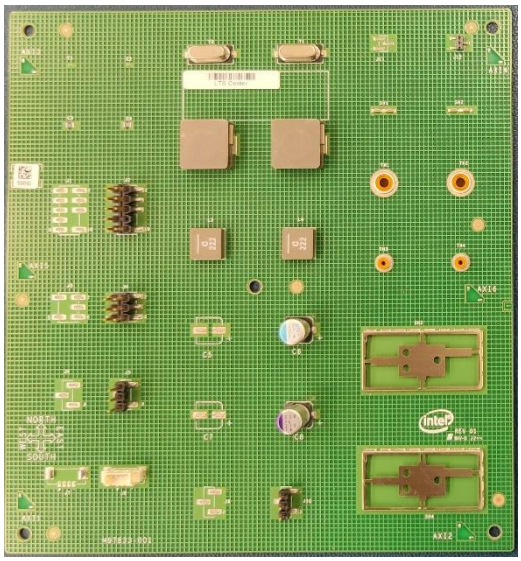
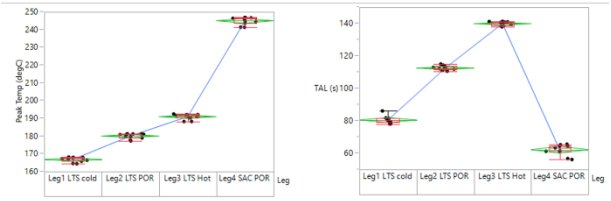


Figure 3. Shear test board compatible with JEDEC size

Leg	Paste	Reflow profile	Stencil thickness	Qty
1	LTS	Cold	3mil	5
2	LTS	Center	3mil	5
3	LTS	Hot	3mil	5
4	SAC	Center	3mil	5



Variability Summary for Peak Temp

	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
Peak Temp	195.7318	30.09891	4.537581	186.5809	204.8827
Leg[Leg1 LTS cold]	166.8709	1.358709	0.409666	165.9581	167.7837
Leg[Leg2 LTS POR]	180.0627	1.461404	0.44063	179.0809	181.0445
Leg[Leg3 LTS Hot]	190.9618	1.532598	0.462096	189.9322	191.9914
Leg[Leg4 SAC POR]	245.0318	2.08399	0.628347	243.6318	246.4319

Variability Summary for TAL

	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
TAL	98.77318	30.19436	4.551971	89.59326	107.9531
Leg[Leg1 LTS cold]	80.49455	2.262164	0.682068	78.9748	82.01429
Leg[Leg2 LTS POR]	112.4964	1.337709	0.403334	111.5977	113.395
Leg[Leg3 LTS Hot]	139.87	1.185791	0.357529	139.0734	140.6666
Leg[Leg4 SAC POR]	62.23182	3.267197	0.985097	60.03689	64.42675

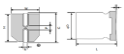
Figure 4. DOE legs for the JEDEC board

RESULTS AND DISCUSSION

A comparison of the max shear force on the 3.81mm tall 3-pin headers sheared off from functional boards assembled under various assembly conditions is shown in Figure 5. Figure 7 indicates that the overall component shear strength is equivalent between LTS paste and SAC paste within the same volume conditions. It can also be seen that the surface finish (OSP vs ENIG) doesn't have a significant effect on the shear strength. There is also no sensitivity of the shear force to volume (3mil vs 4 mil thick stencil) of the solder paste when compared for a particular solder paste.

Figure 6 shows the effect of reflow conditions on the max shear force needed to shear off several components assembled using LTS paste. There is no effect of Reflow peak temperatures and TAL on the shear strength if they are within process window provided by the paste supplier. Most of the components were sheared with the Test Frame shown in Figure 1, but shields and PEM nuts could not be sheared off due to their low profile. A pull test was done on shields and the PEM nuts were torqued as shown in Figure 8. SAC is slightly stronger than LTS for PEM nuts as shown in Figure 9.

Table 2. Components on the JEDEC test board

Component Type Termination Style	Body Size (W x L X H)	Image	Risk
0201 Resistor/Capacitor	0.6 x 0.3 x 0.3mm		Assumed Low risk
0805 Resistor/Capacitor	2.0 x 1.25 x 0.33mm		Assumed Low risk
2 Pins Inductor (L-shape termination)	12.9 x 13.2 x 5mm		Handling risk for breaking the solder joint.
2 Pins Inductor (Bottom termination)	7.5 x 7.5x3.1mm		Handling risk for breaking the solder joint.
Aluminum Electrolytic Capacitor	7.7 x 6.2 x 7.7mm		Handling risk for breaking the solder joint.
Aluminum Electrolytic Capacitor	6.6 x 6.6 x 9.9mm		Handling risk for breaking the solder joint.
2 Pins Crystal	4.8 x 12.5 x 3.8mm		Handling risk for breaking the solder joint.
2 x 5 Pins Connector	7.44 x 11.94 x 16mm		Handling and Plug/unplug risk breaking the connector solder joint.
2 x 3 Pins Connector	7.44 x 7.62 x 16mm		Handling and Plug/unplug risk breaking the connector solder joint.
1 x 3 Pins Connector	2.54 x 7.62 x 16mm		Handling and Plug/unplug risk breaking the connector solder joint.
1 x 4 Pins Plug	2.4 x 9.75 x 4.7mm		Handling and Plug/unplug risk breaking the connector solder joint.
3 Pins Connector	2.54 x 7.62 x 6.86mm		Handling and Plug/unplug risk breaking the connector solder joint.
3 Pins Connector	2.16 x 3.81 x 3.91mm		Handling and Plug/unplug risk breaking the connector solder joint.
Through Hole Standoff M3	Diameter = 5.5mm		Torque screw risk of breaking the joint for heat sink or M.2 assembly.
Through Hole Standoff M1.6	Diameter = 3.0mm		Torque screw risk of breaking the joint for heat sink or M.2 assembly.
Shield Clip M11758-001	6.7 x 0.9 x 1.28mm		Removal of lid from clip risk pulling the clip off
Shield fence	30.91 x 15.28 x 1.4mm		Removal of lid from fence risk pulling the fence off

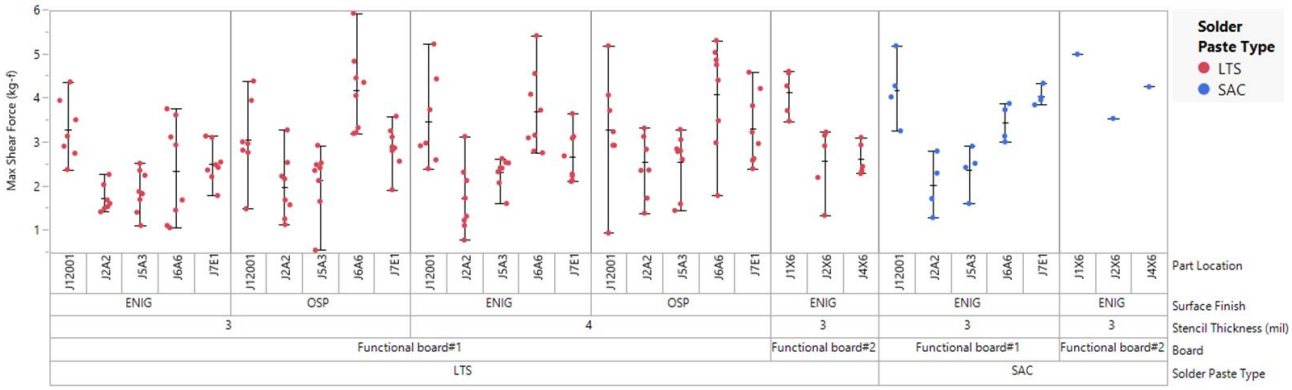


Figure 5. Max shear force on 3-pin headers sheared from the functional boards

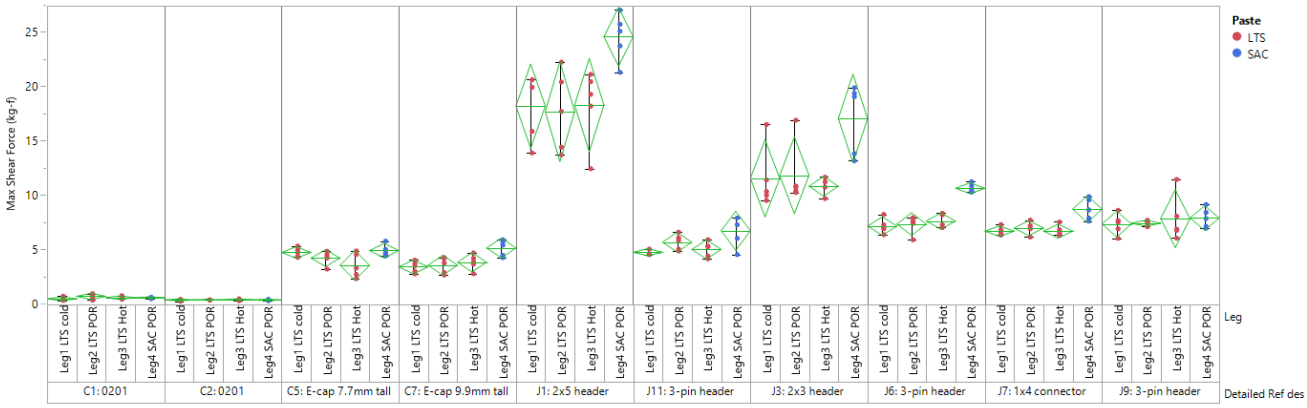
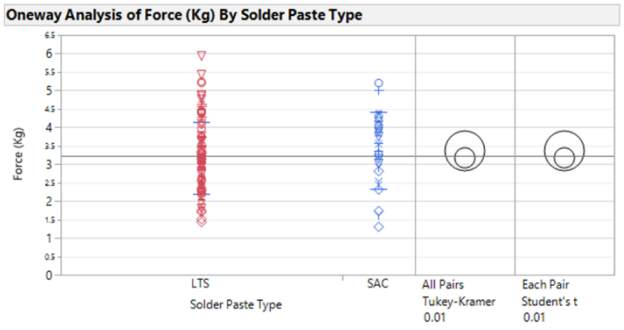


Figure 6. Max shear force on components built with LTS and SAC paste on the Shear test board



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 99%	Upper 99%
LTS	89	3.1716854	0.975266	0.103378	2.8995058	3.443865
SAC	23	3.3613043	1.0447588	0.2178473	2.747246	3.9753627

Figure 7. Equivalence of max shear force between LTS and SAC solder paste

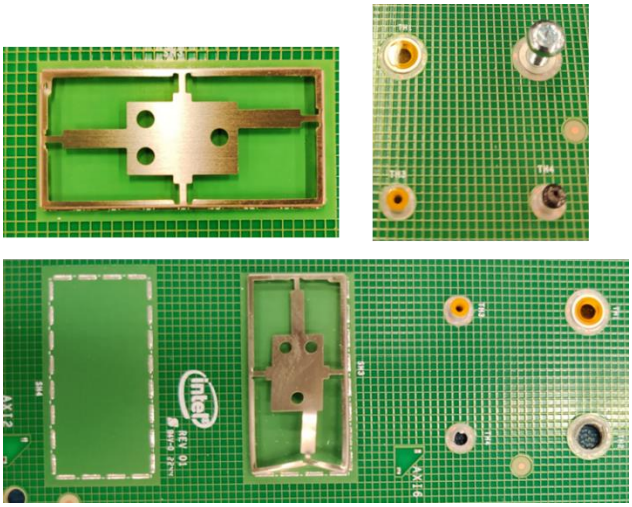


Figure 8. Pull test on Shields and torque test on PEM nuts

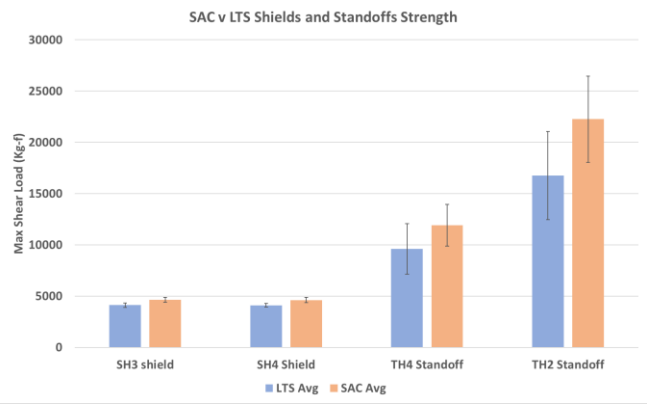


Figure 9. Max shear force on shields and standoffs

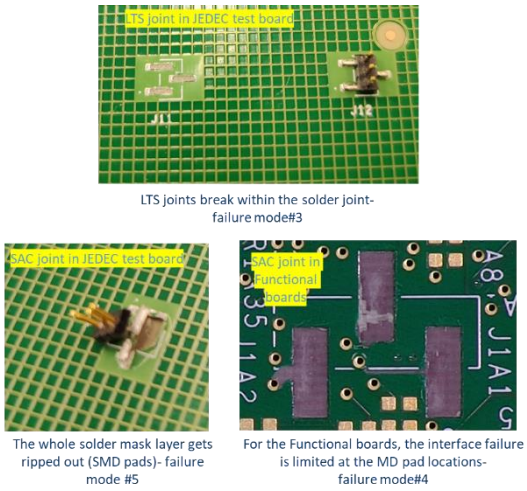


Figure 10. Failure modes of LTS and SAC joints after shear

Figure 10 shows the solder pads for both SAC and LTS after shear failure. Components built with LTS paste showa crack through the solder joint with the remaining solder visible on the pads. The behavior is consistent with both SMD and MD pads. SAC, however, shows a different characteristic of failure depending on the type of pad. For metal defined (MD) pads, the failure location is at the interface between the solder and the pad underneath, while for solder mask defined (SMD) pads, the pad itself gets ripped out from the PCB revealing the dielectric layers underneath. The strength values between LTS and SAC are still comparable even though the mechanisms of failure for both are different. The difference is likely due to the PCB reaching higher temps during SAC reflow and softening the solder mask layer or the Copper pad.

It is worth noting that these JEDEC test boards were tested within a month of being assembled so there was no aging effect of the paste captured by these shear tests.

SUMMARY

Shear testing was conducted on several components such as headers, E-Caps, crystals on functional and test boards. The results show that the LTS has similar shear strength to the SAC joints. There are, however, differences in the failure mechanisms between LTS and SAC. Figure 11 illustrates the five failure mechanisms that are possible upon shearing a component. When the component itself breaks then that failure is represented as Mode #1. Mode #2 occurs when the joint between the component leads and the solder breaks. When the crack propagates through the solder joint, then it is Mode #3. Interface cracking between the solder and the pad is represented as Mode #4. When the pad is pulled off completely from the PCB then it is shown as Mode #5. LTS failures are typically Mode #3 while SAC shows Mode #4 or Mode #5 depending on whether the pads are MD or SMD. Despite the differences between failure mechanisms, the shear strength values between the Sn-57Bi-X LTS and SAC305 solder pastes remain comparable. These results do not apply to all formulations of the Sn-Bi alloys and it is recommended to verify mechanical performance of the LTS paste before using it for any application.

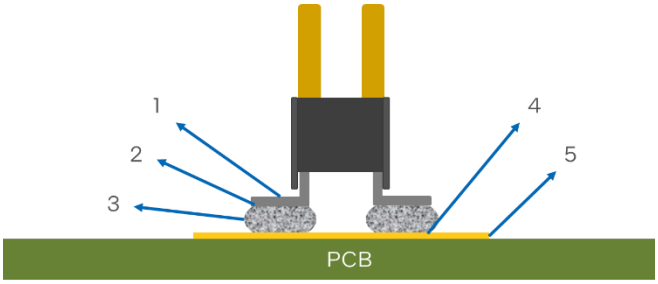


Figure 11. Shearing mechanism based on the location of cracking

FUTURE WORK

There are concerns in the industry on the effect of aging on the shear strength of the LTS pastes. The aging study will be performed using the JEDEC board under the various factors described in this study.

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