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Low Temperature Solder Hybrid Solder Joint Time Dependent Behavior

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ABSTRACT
Hybrid low temperature solder (LTS) joints are created when a component with tin-silver-copper (SAC) solder balls is joined to the printed circuit board with a tin-bismuth based LTS paste. As the industry increases data collection with LTS pastes, several unique phenomena have been noted in hybrid solder joints. A defect mode commonly referred to "ball drift" or "ball shift" has been documented as occurring during thermal cycle testing. As well, very different microstructure development has been seen after isothermal again of hybrid joints using high vs. low silver SAC balls. This paper will review a model to illustrate the source of "ball drift" and will report empirical results from testing designed to confirm the mechanism and highlight a possible mitigation method. Additionally, mechanical strength results will report for high and low silver solder joints assembled with LTS pastes of varying bismuth concentrations and aged for a range of times and different temperatures. Conclusions will be provided for both the "ball drift" mechanism as well as the mechanical performance of isothermally aged hybrid solder joints.

Key words: Solder, LTS, SMT, ball drift, thermal cycle, solder aging, silver content, shear

INTRODUCTION
The concept of soldering a land grid array of pads to a mother board with BGAs (Ball Grid Arrays) has become highly prevalent in the microelectronics industry and has revolutionized the options available for low-cost packaging [1]. The desire for an area array solution stem from the basic premise of a smaller footprint for higher pin count packages. Market opportunities for BGAs have expanded at better than 30% growth rates per year. With an average of 300 pins on each, and an estimated cost of 2¢ a ball, the potential market volume may approach $20B [2]. BGAs today have a huge impact on the roadmap of every aspect of packaging technology. The continuing demand of system miniaturization has been driving the microelectronics industry to the development of consumer electronics that is smaller and faster, with more functionality but at a lower price. The many flavors of BGA packages have made them popular options for graphics, PLDs, DSPs, ASIC, gate arrays and memory packages in that, compared with traditional Surface Mount Technology (SMT) components, they have higher I/O density, lower assembly cost, self-alignment capability during reflow, lower package profile, higher electrical and thermal performance [3]. In response to the increasing demand for higher speed and power of semiconductor devices together with die shrinkage and functional integration, various thermally enhanced BGAs were invented. Some of the examples include, Enhanced BGA (EBGA), Super BGA (SBGA), Ultra BGA, FCCSP, LPDDR etc. [4]. With the complex computing needs for large sets of data processing, along with computing power of the CPU, need for memory storage and memory processing is also a big need in current electronics industry. Memory is widely divided into 2 categories, largely separated between Non-Volatile Memory and Volatile Memory. Within Non-Volatile Memory we have Read Only Memory (ROM) and Read/Write Memory (RWM). Within which we have Mask-Programmable ROM and Programmable ROM along with EPROM and FLASH as the Read/Write Memory options. For Volatile Memory we have Random Access memory such as DRAM/SRAM and Non-Random Access such as FIFO, LIFO and Shift register memory [5]. Dynamic Random Access Memory (DRAM) devices are used in a wide range of electronics applications. Although they are produced in many sizes and sold in a variety of packages, their overall operation is essentially the same. DRAMs are designed for the sole purpose of storing data. The only valid operations on a memory device are reading the data stored in the device, writing (or storing) data in the device, and refreshing the data periodically. To improve efficiency and speed, several methods for reading and writing the memory have been developed. Along with memory needs, there is also a need for robust memory packaging for thermal performance, reliability and low latency performance issues. Several packaging technologies have been developed such as PoP (Package on Package), low cost and high-density performance packaging shown by 2.5D SiP which enables placing memory dies near SoC, Chip Stack (vertical) conventional chip stack using wiring and TSV chip stack, FOWLP (Fan out package) enables several unique features but cost reduction is needed for this packaging technology to be able to deployed at large scale. Some of the most recent packaging technologies include Wire bond (organic substrate), Lead frame, 3D TSV DRAM, Flip Chip, TSV HBM, WLCSP and Hybrid Bonding. There is a vast segment of various markets where applications of high-end memory are needed, e.g., include Datacenter, PC/Client, Mobile, Automotive and Consumer segment. While there is a high demand of memory needs, given the sheer need for large data processing, package sizes for majority BGAs is also increasing which possess various manufacturing challenges. One of the major problems faced by various OSATs and CM for large form factor packages is package warpage at high

reflow temperatures. Package warpage can severely restrict yield issues which becomes a major challenge especially in high volume manufacturing environment where cost per unit of manufacturing, yield loss and rework processes adds major hurdle for CMs.

A cost-effective method to limit these manufacturing challenges lately use of LTS (Low Temperature Solder) has demonstrated some promising results. Low Temperature Solder: Sn-Bi system has advantage where maximum reflow temperature can be limited to ~ 190-200 C in comparison to SAC reflow temperature of 245 C. This reduction of ~ 45-55 C temperature gives major advantage for warpage control which helps alleviate several manufacturing challenges. Reducing this reflow temperature helps reduce warpage and thermal stresses both on the PCB and component which helps increase SMT yields [4]. SMT pass-fail yield is significantly improved, with increased margin of deposited solder paste volume. Advantage of using Low Temperature solder is that it can also be used with off-the shelf BGA components. LTS solder paste can be used to surface mount LPDDR, FCCSP memory packages which have SAC BGAs. This is referred to as a "hybrid" joint where the BGA metallurgy on memory package is SAC (Sn Ag Cu) but the package is reflowed at lower temperature using LTS paste. Given the maximum reflow temperature of the package does not exceed 190-200 C, the SAC BGA does not completely melt but LTS solder paste melts which causes partial Bismuth diffusion in the SAC joint. Given the SAC BGA does not completely melt, the solder joint post reflow solidification temperatures are taller compared to traditional full stack SAC or full stack LTS joints. The difference in solder joint height would depend on the pre-SMT BGA diameter but the advantage gained is that a SAC BGA component can still be surface mounted at lower temperature using LTS paste. This gives manufacturing advantages especially for large form factor packages.

BALL SHIFT PHENOMENON:

While there are advantages of reflowing large form factor packages with BGA metallurgy at LTS reflow temperatures using LTS solder paste, there could also be some draw backs. In this paper we report the phenomenon of "Ball Shift" or sometimes referred to as "Ball Drift" that has been reported as a new phenomenon in microelectronics industry. Ball Shift phenomenon, where BGA joint post stress conditions was observed to be shifted or drifted from the pad locations both at the package side and the motherboard side. Interesting aspect of Ball Shift phenomenon is that post SMT at T = 0, there is no Ball Shift observed on any joints either on the pad side or the package side. This phenomenon is only observed once packages are subjected to thermal cycling. Post temp cycling testing beginning small shift in the BGA pins is observed and during successive progression of thermal cycling, ball drift becomes more and more prevalent where major breakage of the joint from package side and board side is observed. Result in BGA pad breakage results in serious reliability concerns and raises questions to understand the fundamental mechanisms that drive the ball drift phenomenon and beg the question to help identify solution paths and come up with mitigation strategies that can help reduce and perhaps eliminate the phenomenon of ball shift. Figure 1 below shows the LPDDR memory package that was reported to show ball shift phenomenon. X-ray Image taken post stress.

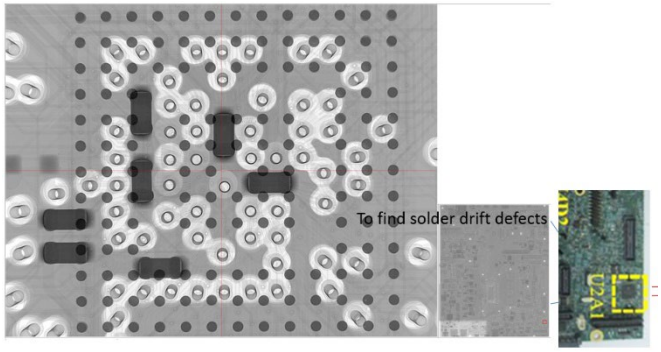

Figure 1: X-ray image of LPDDR memory

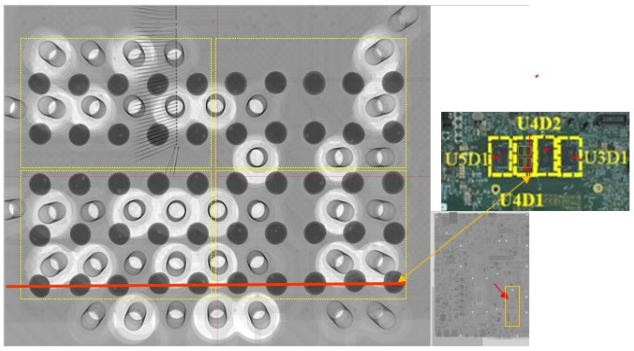

Figure 2: X-ray image showing Ball Shift at package edge

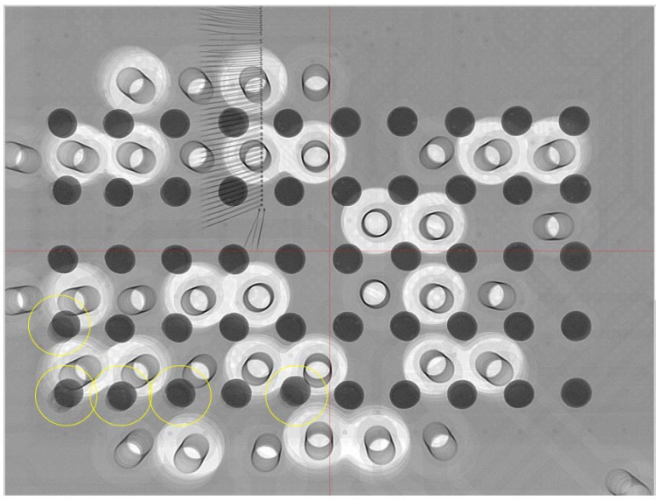

Figure 3: Ball Shift seen highlighted in yellow circles

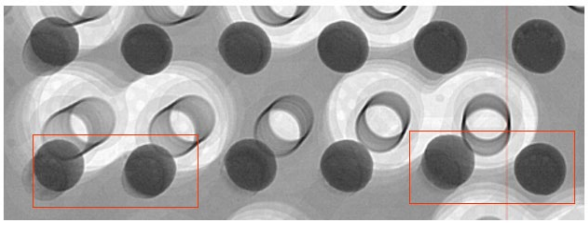

Figure 4: Ball Shift seen highlighted in red squares

Figure 2 shows how the ball shift phenomenon prorogates. As can be seen with a straight red line that the joints have drifted from their axis. This is unusual to observe given the joints post fatigue can break if exceeded over their lifetime, but they would not demonstrate a physical shift from their axis. Figure 3 shows a close-up X-ray image of more joints that show ball shift phenomenon. As can be seen in Figure 3, most of the joints that demonstrate ball shift phenomenon, they exhibit this behavior predominantly on the package edge and or package corner. This was a unique signature given that on the same package, no ball shift was observed for joints near the package center region or package cavity region. This was an indication that that joints within the package cavity or package center region could be insulated from exterior joints and perhaps were not subjected to high shear stress and strain which potentially could have resulted in overcoming the ball shift phenomenon. Figure 4 shows a close-up X-ray image which shows a significant displacement of the joints from their axis. The location of these joints was also the same where joints at the package edge and package corner demonstrated higher ball shift and joints in the package cavity and center region did not show ball shift.

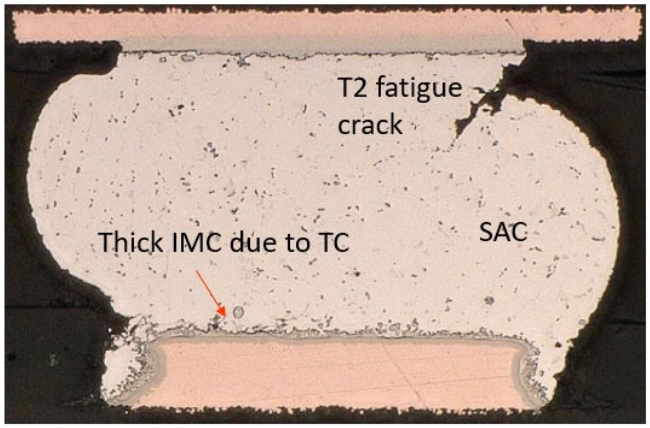

Figure 5: X-section image of joint demonstrating ball shift

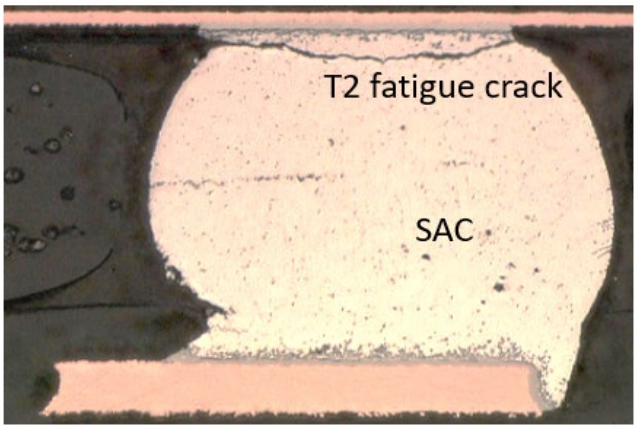

Figure 6: X-section image showing T2 crack due to ball shift phenomenon observed on both package and board side

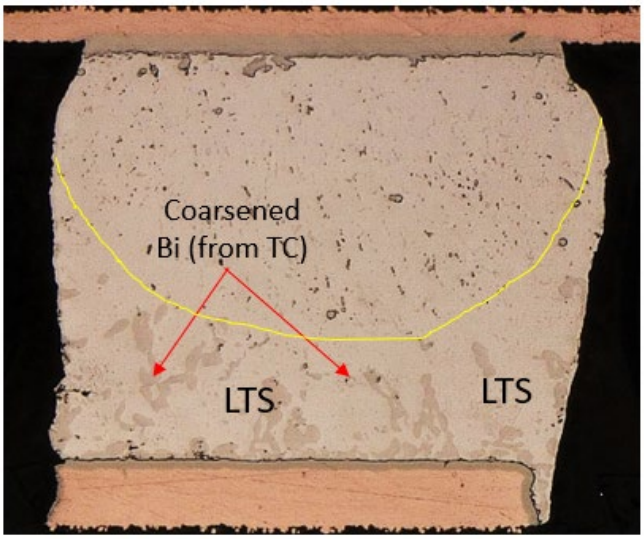

Figure 7: X-section image of a joint that did not demonstrate Ball Shift, i.e., good hybrid joint

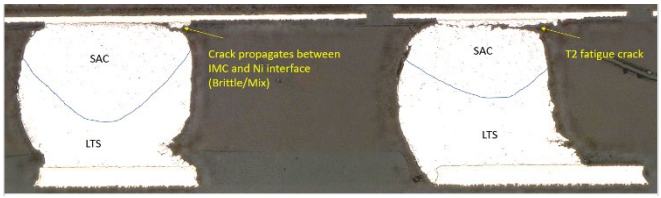

Figure 8: X-section image showing ball shift that resulted in joint crack from T2 interface

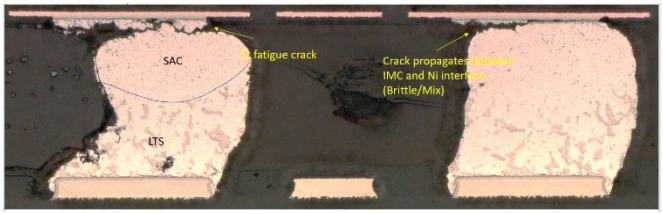

Figure 9: X-section image showing ball shift that resulted in major cracking that occurred at T2 interface.

Figure 5 shows X-section image of a joint that went through temp cycle stress that resulted in ball shift phenomenon. Figure 6 show ball shift as seen on the joint predominantly on the board side and resulted in major shift of the joint which became too strong and resulted in T2 crack. Figure 7 above shows what a good hybrid joint post temp cycle stress would look like. This joint did not result in ball shift phenomenon and hence no ball crack was observed. Important to note that this joint was within the package cavity region, i.e., this joint was not at the package corner or package edge. Given the joints within package cavity region are shielded from outer joints, we believe was the reason why this joint although on the same package did not result in ball shift phenomenon. Figure 8 and Figure 9 demonstrate 2 cases of severe ball drift. As can be seen in both the images the LTS portion of the joint was not drifted as severely when compared to the SAC portion of the joint. It is also interesting to note that the shift in the joint can be observed on either the right side or the left side. This indicates that joint would shift towards either direction that would exert higher pressure on the BGA to drift. These images also show that once a solder joint crack is initiated due to ball shift phenomenon, either at the package interface or the board interface, it would result in severe crack propagation which would eventually result in complete collapse of the solder joint at the given interface manifesting in an open which resulting in severe reliability issues.

SAC VS LTS MATERIAL PROPERTIES:

Given ball shift phenomenon was observed on hybrid joints only and that we did not see this phenomenon full stack SAC or LTS joints or at T = 0, this begged the question to understand the material properties of SAC and LTS solder metallurgies especially at different ends of temperature ranges. Table 1 below shows material property comparison between SAC and Sn-Bi based LTS system. This table shows that at lower test temperature, tensile strength of LTS paste is higher and tensile strength of SAC paste is lower. It clearly shows that tensile strength of LTS paste is ~ 2x more than that of SAC when subjected to lower temperature measurements, in this case lower test temperature was -40 C. Whereas at higher temperature SAC and LTS tensile strengths are comparable. Thus this data helped differentiate the material property facts of LTS and SAC that tensile strength has a substantial impact on LTS at lower temperatures when compared to SAC metallurgy.

Table 1: SAC vs LTS material properties comparison

SAC vs LTS material properties

Paste Composition (wt%)	Melt Temp [ºC]	Test Temp [ºC]	Tensile Strength [Mpa]	Elongation [%]	Young's Modulus [Gpa]	0.02% Proof Strength [Mpa]	0.2% Proof Strength [Mpa]
Sn-4Ag-0.5Cu (SAC)	217 - 229	-40	67.9	44	54.1	20.9	33.8
		25	47.9	49	46.6	19.8	28.6
		85	30	50	40.1	13.7	22.1
		125	20.5	63	35.7	12.2	16.2
Sn-40Bi-0.5Cu-0.03Ni (LTS)	139 – 174	-40	127.2	15	44.1	43.4	54.6
		25	76.4	47	39.2	24.8	39
		85	37.2	213	25	10.7	23.6
		125	17.9	202	18.8	5.9	13.4

BALL SHIFT MODELLING ASSESSMENT:

To understand the impact of different material properties for both SAC and LTS, modelling assessment was performed where shear behavior of a full stack SAC system was compared to a hybrid joint system (SAC BGA + LTS paste). Figure 10 above shows when package is under stress condition, in this case modelling assessment was performed for temperature cycling stress, that when the joint is subjected to hot part of the cycle, the package is pulled towards the package center and when the joint is subjected to cold part of the cycle, the package side is pushed away from the package center. This shear behavior study was to evaluate the impact of movement of the joint would have on SAC and LTS metallurgy systems. Key assumptions that were made for this study was that effective CTE of the package is lower than the effective CTE of the board. Also, the sheer magnitude on the joint is increased with increasing CTE delta and the package size.

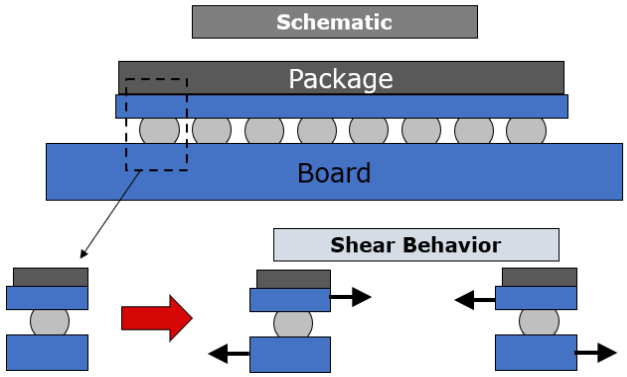

Figure 10: Shear Behavior modelling assessment under temp cycle stress conditions

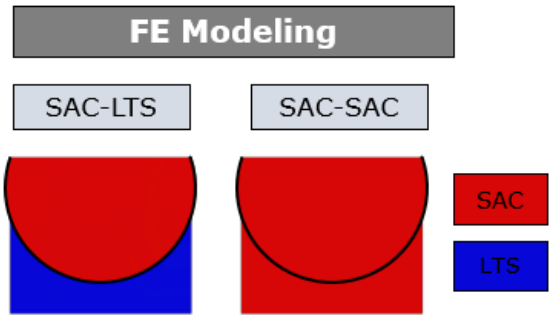

Figure 11: FE modelling assessment peformed for full stack SAC joint and hybrid joint (SAC BGA + LTS paste)

Figure 11 above shows that systems that were used for modelling assessment. Two systems were used to understand the ball shift phenomenon. A full stack SAC system, i.e., SAC BGA + SAC paste and a hybrid stack system, SAC BGA + LTS paste were used for this study.

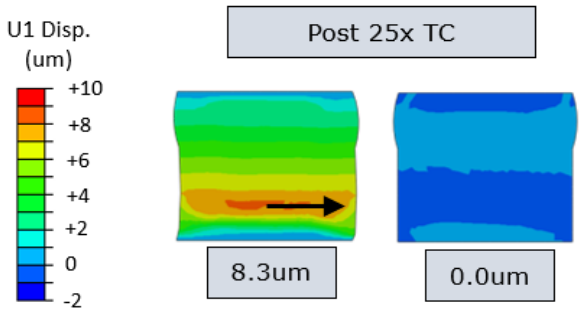

Figure 12: Post thermal cycling assessment for full stack SAC and LTS system

Figure 12 above shows the post temperature cycling modelling assessment results. Thermal cycling assessment of 25x cycles was performed. Temperature variations of range from – 40 C to +100 C was used for stress assessment. This temperature range is standard TCT (Temp cycle test) requirement for SJR (Solder joint reliability) study performed for majority BGA SJR evaluations. As can be seen in Figure 12, a single solder joint simulation with 25x temperature cycles shows that the SAC-LTS hybrid solder joint system drifts towards the package center. This was the same behavior as observed in the actual failing mode highlighted in images above. Full stack SAC (SAC BGA + SAC paste) system did not demonstrate this behavior. This simulation study clearly indicated that given the material property differences between LTS and SAC a drift in a hybrid system is primarily due to metallurgical properties of LTS solder. This begs the question why such drift is not observed in full stack LTS system. From our studies, we believe that when LTS is subjected to extreme low temperature ranges, it exhibits high tensile strength, however when the full stack LTS system is going through a hot part of the temperature cycle, it has inherent material property to recover that extreme high tensile strength it was subjected to under lower temperature part of the cycle. i.e., full LTS metallurgy when subjected to low temperature and its increase in tensile strength can be recovered during the hot part of temperature cycle. In contrast to this, in a hybrid system, when the LTS joint is subjected to lower part of temperature cycle increasing its tensile strength, when this system goes through hot part of the cycle, given SAC system and LTS systems have comparable tensile strengths at high temperatures, the amount of tensile strength gained by LTS portion of the joint in lower temperature part of the cycle, becomes irrecoverable. LTS portion remains in a state of extreme high tensile strength and cannot recover to its original state. This induces tension on the joint which only increases during numerous repetitions of thermal cycling at hot and low temperatures.

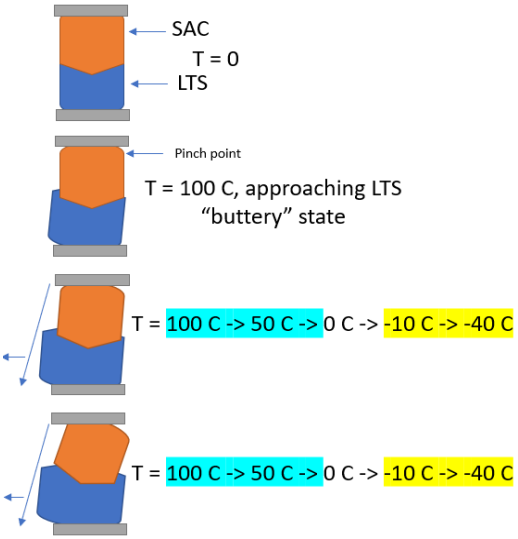

FIGURE 13: Schematic of ball drift hypothesis
Figure 13 shows the schematic of ball shift hypothesis.

EMPIRICAL DATA COLLECTION:
To understand various contributors to ball shift phenomenon, such as CTE mismatch between package and PCB, tensile strength material property differences between LTS and SAC, different type of memory packages, impact of outer joints shielding inner joints where ball shift phenomenon is not observed, we performed empirical data collection on 2 memory packages. As seen in Figure 14 below a 4-UP JEDEC layout board was designed to perform temperature cycle studies and evaluate above mentioned variables and its impact on ball shift phenomenon. Board was 36 mils thick with an 8-layer stack up. This board was designed with intent to perform both temperature cycle and shock data collection, if needed. Temperature cycle conditions were chosen to be – 40 C to + 100 C. These are standard TCT conditions used for BGA SJR (Solder Joint reliability) evaluations. To understand impact of glue in restricting the shear drift experienced by the solder joints, we included boards with and without corner adhesives.

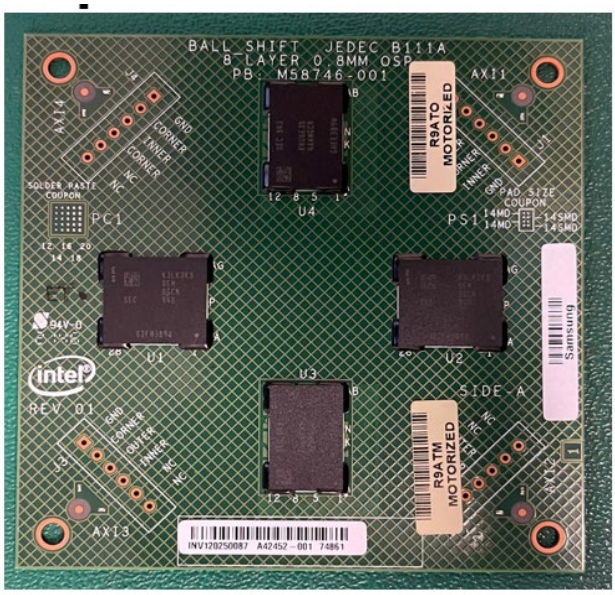

Figure 14: JEDEC board designed to perform Ball Shift phenomenon studies

Table 2: Ball Shift DOE empirical data collection results

Vendor	Package	Corner Glue	CTE1	Ball Shift observed
A	200	No	8.5	Yes
A	496	No	13	No
B	200	No	12.7	Yes
B	496	No	9.9	Yes
B	200	Yes	12.7	No
B	496	Yes	9.9	No

2 memory suppliers were selected. 2 package configurations were used. One package had total pin count of 200 and 2nd package had total pin count of 496. Varying CTE range was used to evaluate impact of CTE on ball shift phenomenon. CTE ranging from 8.5 to 12.7 were selected for this study. As seen in table 2 above, post ~ 1000 temp cycles, severe ball shift was observed on both memory suppliers' packages. Ball shift was observed on packages with both 200 and 496 pin count. It was also interesting to observe that ball shift was observed on low end of the CTE range of 8.5 along with high end CTE range of 12.7.

CONCLUSION: This study demonstrated that mode CTE is not a definitive variable for ball shift phenomenon. Key interesting observation we found was that while given the metallurgical properties of LTS and SAC system, ball shift can be observed in LPDDR and WLCSP packages, however, a mitigation strategy of adhesives application can be employed to over the ball shift phenomenon.

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