Increased Reliability of Quad Flat No Lead (QFN) Wettable Flank Connections by Immersion Tin Plating

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ABSTRACT

The quad flat no lead (QFN) package connects the integrated circuit (IC) to the printed circuit board (PCB). The exposed copper on the side edges can be a weak point in the long-term reliability of the connection and also lead to the detection of phantom failures in the automated optical inspection (AOI). In order to achieve a 3-dimensional solder connection to the PCB, the preferred approach would be that the solder joint is not only formed between the QFN bottom side and the PCB but also includes the wetting of the QFN flanks. Immersion tin plating offers the possibility to create fully wettable flanks by covering exposed copper at the QFN side walls with a plated tin layer. Nevertheless, there are concerns that immersion plated tin layers might be not enough to pass the shelf-life requirements and heat treatment due to the formation of the Cu/Sn IMC.

As the lead frame material differs from the copper substrates as used in standard PCB applications, the immersion tin plating process requires dedicated adjustment. The focus of this study is to investigate the reliability of the immersion tin layers plated by a tailored immersion tin process for QFN flank plating. The tin-plated surface of the QFN flanks is investigated in regard to its soldering performance. This is realized by applying soldering and aging criteria as defined by the target industries. The plating process is tailored to the QFN application and includes specific pretreatment steps to prepare the copper alloy for the immersion tin plating. The properties of the plated immersion tin layers are investigated as well as potential impact of the immersion tin plating process on the electrolytic tin layers covering the QFN top. As tin layers in general are suspected to bear the risk of whisker formation as long as they are not soldered directly, this has been considered in the investigation as well. To tackle this risk, the impact of a whisker mitigating additive is also studied and presented.

The soldering performance after different aging conditions is evaluated and correlated to the formation of the intermetallic compound (IMC) after aging. As conclusion it can be stated that the immersion tin coverage of the QFN side flanks allows a enhanced solder wetting and solder joint formation whilst an additionally significant benefit is to enable the possibility of automatic optical inspection.

Key words: QFN; Surface finish; Solder Joint; Immersion tin; IMC.

INTRODUCTION

Immersion tin is a surface finish which is well established in the PCB industry and well trusted in the automotive industry due to its high reliability. In the automotive market the use of QFN (quad-flat no leads) packages becomes of increasing interest due to its flexible form factors, size, scalability, and thermal dissipation capabilities. One step for success has been the side wettable flanks, which provide a reliable solder joint connection to the PCB and enable an automated inspection of the solder joint and solder joint quality. The bottom side of the QFN is usually covered with electrolytic tin and the exposed areas with the copper flanks require additional treatment to enable the solderability of the flanks. Without further treatment copper oxides are built which inhibit the solder wetting so that in such case only 2-dimensional solder joints are formed. To achieve a better reliability, the industry looks into solutions to increase the wettability of the flanks leading to the formation of 3-dimensional solder joints. The plating with immersion tin provides a robust and well solderable surface finish for the wettable flanks which can ensure the solder to wet the flanks, for a reliable joint and allow the judgement of the solder joints by automated inspection.

PRETREATMENT AND IMMERSION TIN PLATING

In the QFN manufacturing the final step is a singulation step which can be either dicing or punching. During this step the flanks can get contaminated by tin smear or molding residues which stick on the surface and cannot be removed with standard pre-clean systems for PCBs. Therefore, the cleaner and microetch are specifically tailored to remove tin and mold residues and level the copper alloy of the lead frame material. One of the factors impacting the leveling performance of the copper is the ration of Chloride and Copper in the etching solution. In the graph in figure 1 the impact of varying the etch parameters is plotted versus the relative surface area increase (RSAI). It shows that the most inconsistent performance for the activator step can be observed for the low pH value. At a pH of 7.9 the overall roughness remains high in particular for the low Cu:Cl ratio. This effect is even more pronounced when the etch is operated with air agitation. For pH 8.2 and 8.4 a consistent performance can be observed leading to comparable etch attack for all tested conditions of the working range.

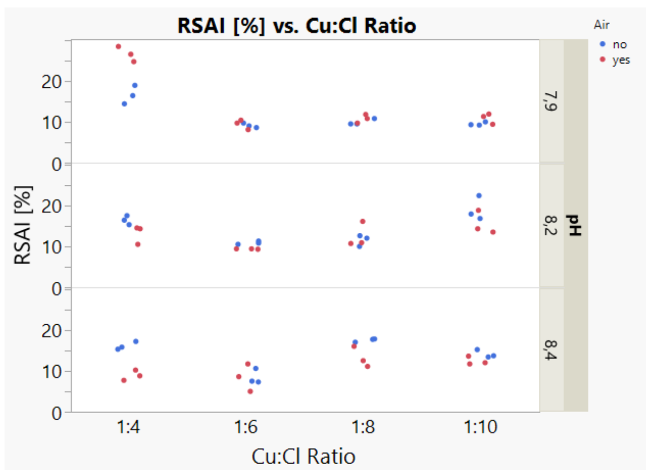
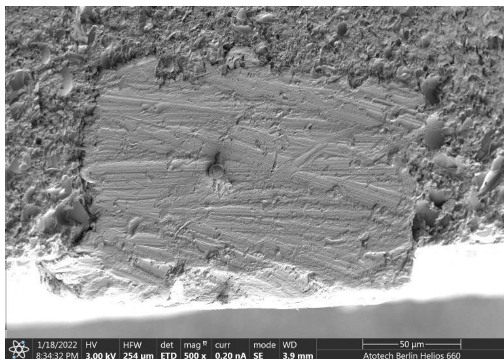


Figure 1: working range evaluation of microetch step

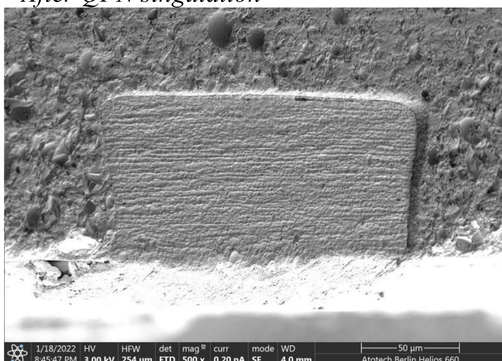
In Figure 2 the copper alloy surface right after the the dicing step (a), after the cleaning step is shown. The cleaning includes a pre-clean and the microetch step (b). Picture c shows the side flank after tin plating (c).

After the precleaning the copper surface appears even, scratches and smear residues from the separation process are removed.

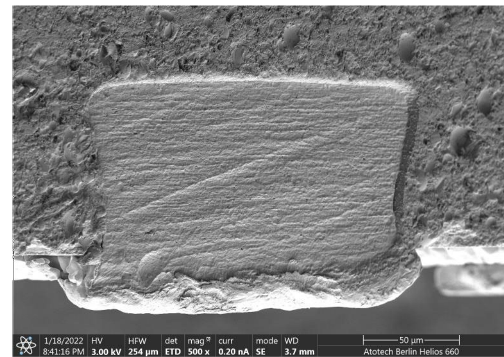
In the immersion tin plating process the side flanks are covered with the immersion tin forming a dense tin layer covering the full pads on the QFN side wall.



a) After QFN singulation



b) After cleaning and microetch



c) After tin plating

Figure 2: pretreatment and tin plating of QFN side flanks

After the tin plating process post treatment solutions can be applied to prevent any discoloration of the tin layers in the later assembly processes and create a hydrophobic surface for an additional protection of steam aging.

SOLDERING TESTING AND IMC FORMATION

To confirm the capability of the tin layers to improve the solder wetting and enable the formation of the 3-dimensional solder joints, the solder wetting is tested by immersing the QFN coupons into liquid solder and evaluate the surface coverage of the side pads with solder. The coupons are dipped into the solder with an angle of 45° for 5 seconds. This test is performed after a thermal pre-aging of 8 and 16 hours at 150°C and a steam aging test at 93°C for 4 and 8 hours. The Graph below (figure 4) shows the result comparing the performance of an immersion tin process dedicated for QFN plating compared to a standard immersion tin process for PCB applied on QFNs.

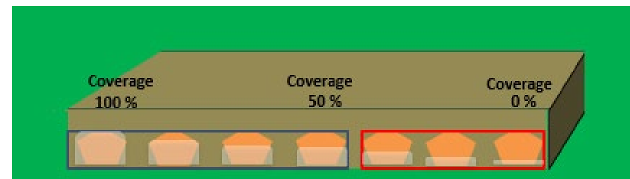
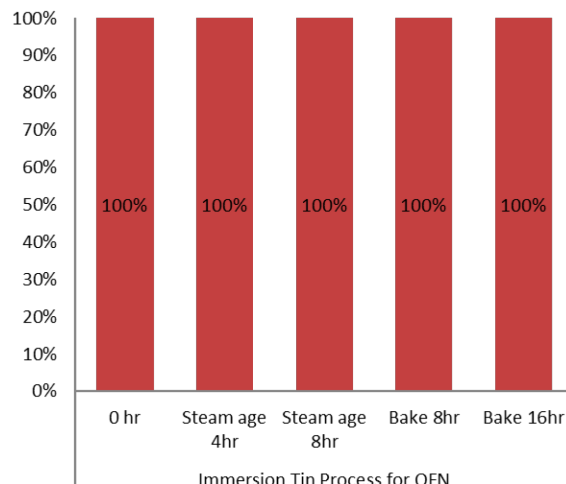


Figure 3: acceptance criteria for solder wetting of QFN side flanks



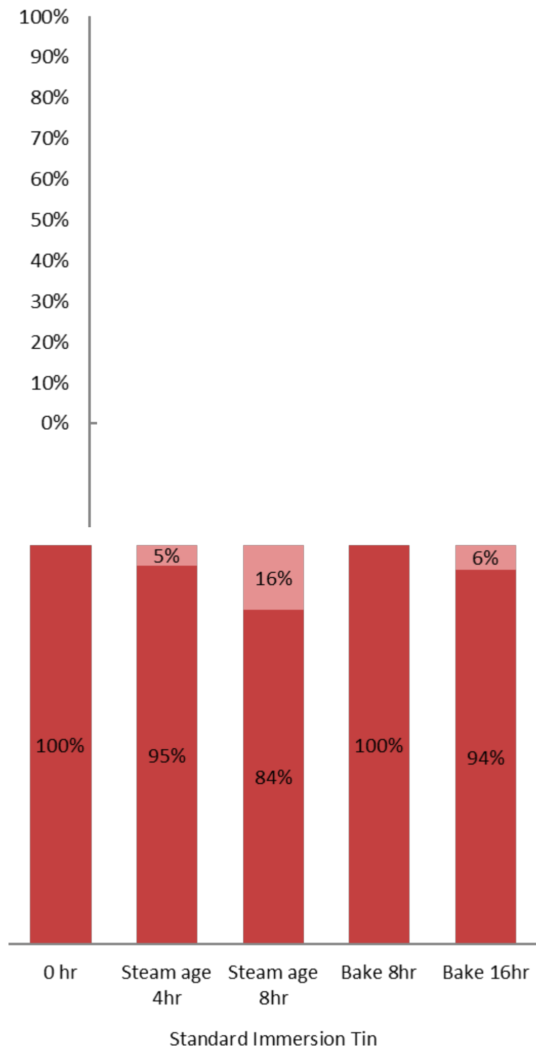


Figure 4: solder wetting of the QFN side flanks with different immersion tin finishes

The pads with a solder coverage of minimum 50% and larger are acceptable, the pads with a coverage of less than 50% are rejectable. Exemplary images of the soldered side flanks are shown in Figure 5. The picture shows the soldered pads after 16h baking at 150°C and after storage for 8h at 93°C and 93% relative humidity.

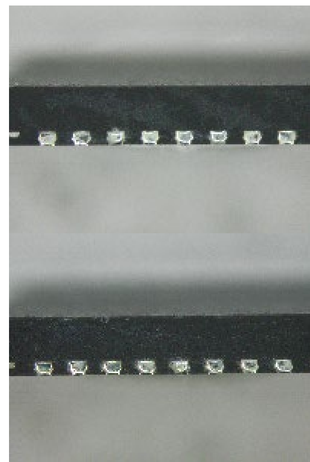


Figure 5: exemplary images of the solder wetting after 16h baking at 150°C (left) and 8 h at 93°C/93% RH (right)

The results confirm that the immersion tin process designed for the QFN side flanks can achieve a significantly better soldering performance than an immersion tin process for PCBs adopted for QFNs.

As during the aging of immersion tin layers, the thickness of the intermetallic compound increases and leads to a lower content of free tin, this often is considered as critical for the solderability of the tin surface. Storage tests have been conducted to study the growth of the intermetallic compound over time depending on the substrate alloy. For this the tin layer have been plated on EFTEC 64T and C194 alloy. The composition of the two alloys is given in table 1.

For all conditions an overall thickness of 1.5 µm tin was deposited and subjected to thermal and steam aging at 150°C and 93°C and 93% relative humidity. The result of the IMC and free tin thickness is shown in the figure below – the thickness is stated in µm where pale blue reflects the free tin and dark blue the IMC:

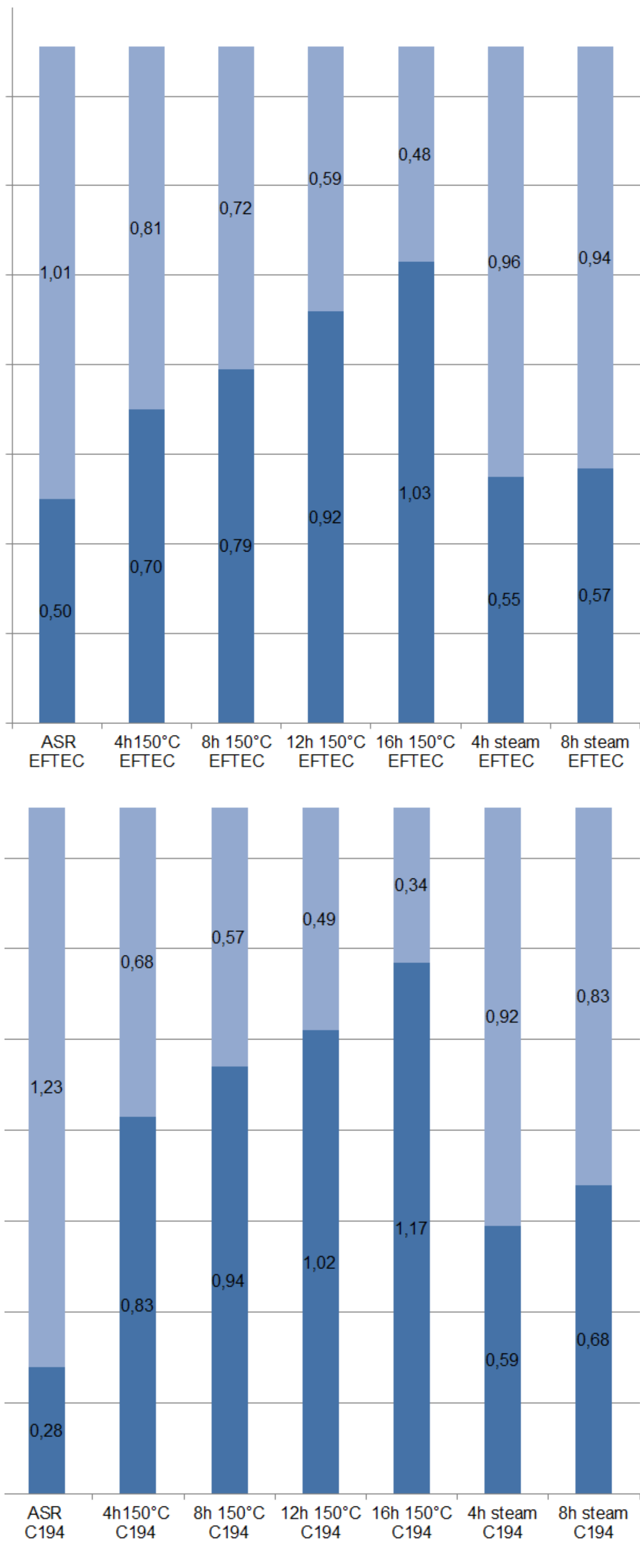


Table 1: alloy composition in %w/w

	Cu	Cr	Sn	Zn	Fe	P
EFTEC-64T	99.25	0.3	0.25	0.2		
C194	Min 97			0.05-0.2	2.1-2.6	0.015-0.15

The results show that the IMC formation is driven by temperature in the first place. The IMC growth is linear over time for the storage temperature of 150°. After 4h at 150°C approximately half of the tin thickness is consumed by IMC. The IMC formation is slower for the humid aging at 93°C where at the same time about 40% of the tin layer are converted to IMC. It also shows, that even after 16 hours at 150°C still 25 – 32% remain to be free tin to ensure a good solderability. The impact of the alloy material is low and leads to approximately 10% more free tin on the EFTEC 64T material.

PLATING IMPACT ON ELECTROLYTIG TIN

As the immersion tin process is a process step being applied additionally to the electrolytic tin plating of the QFN bottom areas, there is a potential risk that the additional plating step can attack or change the electrolytic tin deposit. Therefore, SEM investigations of the surface structure of the tin deposit have been performed to check the impact of each process step of the immersion tin plating process on the electrolytic tin deposit. The pictures in figure 5 show the crystal structure of the electrolytic tin deposit after the pretreatment step, the immersion tin plating, and the post treatment. The crystal structure is comparable for all samples and no attack to the electrolytic tin layer can be observed.

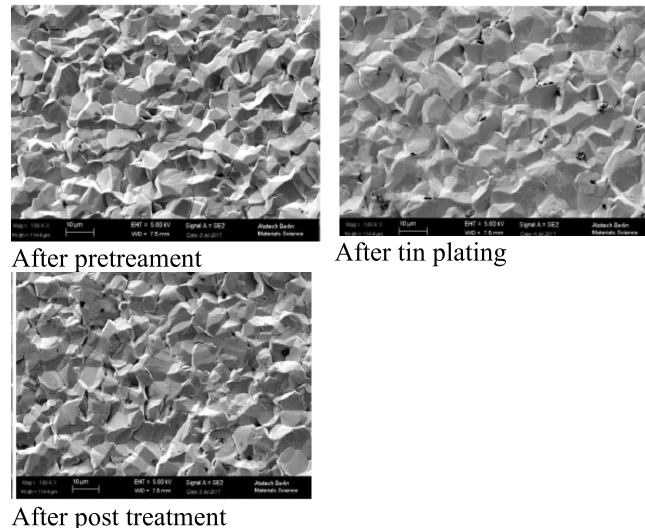


Figure 6: SEM surface images of the electrolytic tin after the immersion tin process

WHISKER MITIGATION OF IMMERSION TIN

Tin layers are known to have a risk for whisker formation which can be either related to the assembly process like press fit application where stress is applied to the coating or to the deposited layer itself. In this case the formation of the

intermetallic compound in the immersion tin deposit leads to the buildup of internal stress in the tin deposit which may lead to the formation of whiskers to reduce the stress.,
To mitigate the whisker formation in the immersion tin deposit, an additive is added to the plating solution, which leads to a co-deposition of Ag in the layer. XEDS (energy dispersive X-ray spectroscopy) mappings of the tin deposit confirmed that the Ag accumulates at the tin grain boundaries. As these are the preferred locations where whiskers form and grow, the incorporation of Ag inhibits the tin migration and by that formation of the whiskers.

In figure 7 and 8 the XEDS mapping, and TEM cross section are shown where the location of Ag in the immersion tin layer can be identified.

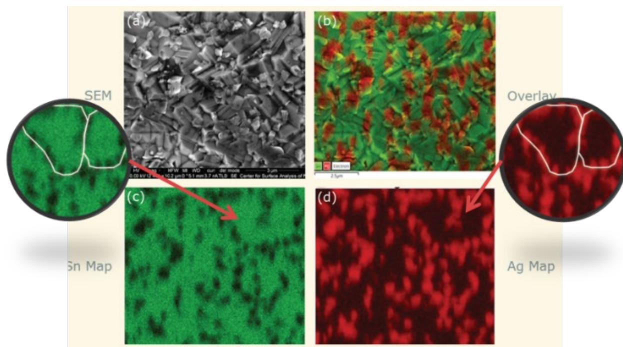


Figure 7: XEDS mapping of immersion tin layer with Ag-additive

The mapping shows, that the Ag is not homogeneously distributed over the full area but is preferably present at the boundaries of the tin crystal grains. The TEM cross section in Figure 8 shows Ag_3Sn grains at the tin grain boundaries, which can act as barriers for the tin migration along the boundaries.

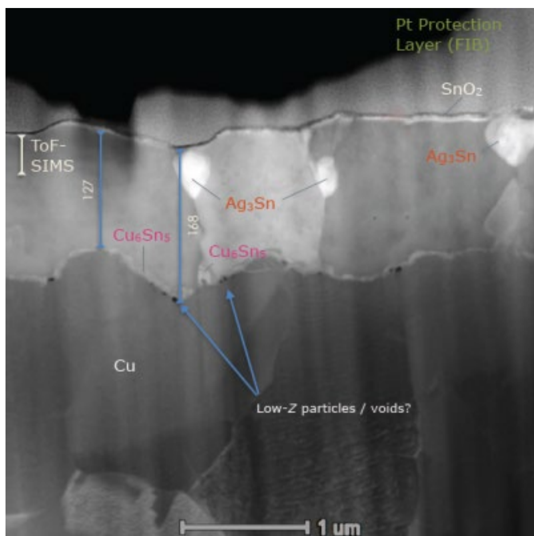


Figure 8: TEM cross section of immersion tin layer with Ag containing anti-whisker additive.

This method of whisker mitigation has proven to work for years already in the PCB industry. It has no negative impact on the solderability of the tin layer and can be monitored in the plating process to ensure consistent layer composition. To check the impact of the anti-whisker additive on the whisker formation, whisker evaluation has been performed after varying storage times. Table 2 gives an overview on the rating criteria, which were applied for the evaluation.

Table 2: Whisker rating criteria

Rating	Whisker size [µm]	Whisker amount
0	0	0
1	≤ 10	≤ 5
2		≤ 10
3		> 10
4	≤ 20	≤ 5
5		≤ 10
6		> 10
7	> 20	≤ 5
8		≤ 10
9		> 10

For the evaluation the tin layer was plated on a test substrate and the whisker evaluation performed after storage times of up to 245 days. Various concentrations of Anti-whisker additive concentration were checked, and it could be confirmed, that already a concentration of 30 ml/l additive solution in the tin electrolyte could lead to a significant and sufficient suppression of the whisker formation. Increased content of additive could further improve the performance for the long storage times.

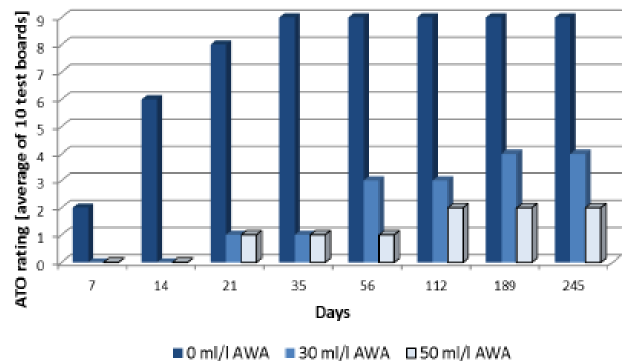


Figure 9: impact of anti-whisker additive on whisker formation after storage

SUMMARY AND CONCLUSION

In this study an immersion tin plating process is discussed, which can improve the formation of three-dimensional solder joints of QFN to enhance the solder joint strength and ease the AOI inspection of the assembled QFNs. The process consists of a dedicated pre-clean system to clean the QFN side flanks after the separation process and ensure a homogeneous tin plating. The tin deposit on the side flanks provides good solderability even after thermal or steam aging which correlates with sufficient free tin remaining after the

IMC formation. The single process steps were checked on their impact on the electrolytic tin deposit of the QFN bottom pad and no negative impact could be detected. To prevent the formation of whiskers which are a known risk for immersion tin deposits, an anti-whisker additive is introduced which deposits at the grain boundaries of the tin deposit and by that inhibits the formation of tin whiskers.

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