Impact of PCB Design, Materials, and Manufacturing Process on PCB BGA Land Pattern Warpage and SMT Yield

Satyajit Walwadkar, Reginald, Lai,Weston, Roth, Alexander Huettis, Samuel Oladji, Juan Landeros, Behrooz Shamsodini , Srinivasa Aravamudhan
Intel Corporation
OR, USA,
Satyajit.S.Walwadkar@intel.com

ABSTRACT
Printed circuit boards (PCB) are considered as the backbone of today's modern electronic devices. PCBs are comprised of alternate layers of conductive and insulating material and serve as a foundational building block for most devices. Electrical interconnects in PCBs are developed by stacking and laminating multiple tightly spaced interconnected conductive layers to form a multi-layer PCB. Manufacturing of a multilayer PCB is complex and involves lamination, drilling and outer layer finishing processes. A typical, type 4 multi-layer PCB undergoes multiple lamination cycles in comparison to a relatively less complex type 3 multi-layer PCB which only needs a single lamination cycle. A limited understanding exists of the impact of the PCB lamination process on PCB ball grid array (BGA) land pattern warpage and surface mount technology (SMT) yield.

This paper discusses the influence of the PCB design parameters, PCB materials, and PCB lamination process on PCB warpage. Both thick and thin PCB cases are presented to capture manufacturing process variability on Type 3 and Type 4 PCBs. Non-destructive metrology was used to quantify and establish incoming PCB land pattern warpage window. SMT yield performance of a BGA package under low temperature solder (LTS) assembly conditions are evaluated on these PCBs to validate incoming PCB land pattern warpage window and to develop a strong understanding of PCB lamination process impact. Finally, recommendations are provided on PCB designs, material selection, and manufacturing optimization to help reduce PCB warpage and maximize SMT Yield.
Keywords: PCB, HDI, lamination, BGA, SMT, LTS

INTRODUCTION
Today's markets are driven by new electronics applications that require higher performance at lower costs to benefit different market segments such as consumer, medical, military, automation, etc. These needs have pushed devices to become smaller, complex, and more efficient as dictated by Moore's law [1]. PCBs which serve as the foundation for such devices must keep up the pace and are constantly faced with higher demands for component, conductor density, speed, bandwidth, and layer counts on a routine basis. This puts a significant burden on the manufacturing processes used to produce PCBs [2]

PCBs are electronic boards with embedded metal circuits that connect different components on the device [3]. PCBs are designed using commercial CAD software to meet the component's electrical demands. While designing PCBs, design for manufacturing (DFM) rules and adherence to guidelines and best practices are typically followed. PCB designs are then converted to working panel designs by PCB suppliers to manufacture PCBs in high volume manufacturing (HVM) process in a cost-efficient method. Manufacturing of the panels is done through appropriate material selection and an assembly process comprising of lamination, drilling, and plating to fabricate the PCB. PCBs in working panels are then depanelized to produce desired PCBs.

The lamination process forms the backbone of PCB manufacturing. It utilizes building blocks of PCB materials such as core, prepreg, and copper foils. These material sets are assembled into stacks of desired thickness and configurations as dictated by design and then pressed together to create a final multilayer PCB. Simple PCB designs, such as Type 3 PCBs are manufactured in a single lamination process step. Complex PCB designs such as Type 4 PCBs that utilize microvias and buried via networks that drive complex internal routing undergo a multi-lamination process. In a multi-lamination process, the build-up of individual layers is pressed sequentially to ensure conductor routing design complexities remain defect free during manufacturing. A limited understanding exists of the impact of the lamination process on the overall PCB warpage and more specifically the PCB BGA region warpage.

The literature survey doesn't offer any valuable insights into understanding the impacts of the lamination process on PCB warpage. This is partly due to the non-standard nature of PCB designs. Custom modeling studies [4,5] done to remain cost-effective show some impact due to internal residual stresses, curing shrinkages, and pressure effects on PCB deformation. However, these studies do not offer realistic design and manufacturing solutions that can be implemented to overcome PCB warpage effects. Most of the attempts that are made to fix PCB warpage problems in SMT by using external means such as pallets and fixtures are discussed in one such study [6]. This approach is extremely time and resource intensive and may not help to completely address the PCB warpage issue.

This paper highlights the source of the PCB warpage issue. Both thick and thin PCB designs involving single and multi-lamination process steps and their impact on PCB warpage are discussed. SMT impact is studied for both these designs and recommendations are provided for design, material, and manufacturing areas to help address the PCB warpage issue.

PCB TV DESIGN AND MANUFACTURING

6 PCBs were designed to study the impact of PCB design on PCB BGA land pattern warpage and SMT yield. PCB designs A, B, and C were created on a 22-layer thick PCB with a large BGA Form Factor and had 3 BGA footprints per PCB. PCB design D was created on a 10 layer thin PCB with a small BGA Form Factor. PCB designs E and F were SMT test vehicles (TVs) for design D. They had further reduced layer count and thickness to improve the yield signal. PCB designs D, E, and F had 1 BGA per PCB with a smaller BGA footprint as shown in Figure 1. BGA footprints were identical within each thick and thin PCB design. SMT assessments were performed on limited PCB designs in each category. Details of PCB design configuration and form factor used for this study are shown in Table1.

Table 1. PCB TV designs used in the study.

S/N	PCB Design Name	PCB Type	Thickness, Layer Count	BGA Type	Purpose
1	A	3	0.125", 22	Large – 62 mm x 72 mm	SMT Yield Assessment
2	B				Manufacturing Influence
3	C				SMT Yield Assessment
4	D	4	0.024", 10	Small – 23 mm x 19 mm	Manufacturing Influence
5	E		0.020", 8		SMT Yield Assessment
6	F				SMT Yield Assessment

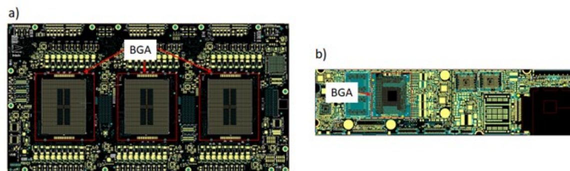

Figure 1. a) PCB design A, B, and C with large form factor BGA with 3 BGA regions b) PCB design D with small form factor BGA with 1 BGA region.

PCB Design and Layout

Commercial PCB software was used to design all the PCB form factors. During PCB design, special attention was given to track layer pair copper balance at the PCB level and PCB BGA region level. Copper balancing was determined by comparing the absolute value of the difference in copper densities between symmetric layer pairs in the board stack up. Figure 2 elaborates the symmetric layer pairs for an 8-layer board design, which was also extended to a 22-layer PCB design. A layer pair with ≤ 10% copper density difference is deemed balanced, and a copper density difference of > 10% is deemed unbalanced. PCB designs A and B have different functions and hence design A had unbalanced copper density within the stack up, whereas design B had balanced copper layers.

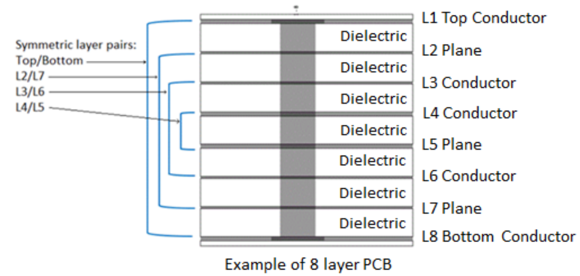

Figure 2. Layer pair balancing procedure followed during designing of the PCB TVs.

A third board, design C, was a modified version of design A with an intent of fixing the unbalanced copper layer pairs within the board stack up. This was achieved by changing the metal-to-metal spacing by layer, allowing for suppression of non-functional pads (NFP) by layer, and changing routing layers to provide a more uniform distribution of copper by layer. As a result, design C had all symmetric layer pairs on the board with a balanced copper density difference of less than 10% as shown in Figure 3. The largest improvements in copper balancing were for layer pairs: L2-L21, L4-L19, L8-L15, and L10-L13.

Layer Pair\PCB Design | PCB Design A | PCB Design A BGA | PCB Design B | PCB Design B BGA | PCB Design C | PCB Design C BGA

L1-L22, L2-L21, L3-L20, L4-L19, L5-L18, L6-L17, L7-L16, L8-L15, L9-L14, L10-L13, L11-L12

Layer Pair Balance < 10% Layer Pair Balance > 10% upto 50%

Figure 3. Results of copper balancing density (%) by symmetric layer pairs for designs A, B, and C. The improved layer pairs with less than 10% offset are highlighted in green over red which had offset between 10% and 50%.

Designs D, E, and F had specific power delivery requirements and being thinner had to utilize any layer stack-up construction. The PCB copper density for Design D was unbalanced with each mirrored layer alternating positive and negative in the layer offsets that were greater than 10% as captured by red colored cells in Figure 4. Copper distribution in the BGA land pattern had a similar offset pattern as the PCB. However, the copper density was more unbalanced with layer offset values higher than the entire PCB.

Layer Pair\PCB Design	PCB Design D	PCB Design D BGA		
L1-L10	> 10% upto 50%	> 10% upto 50%		
L2-L9	< 10%	< 10%		
L3-L8	> 10% upto 50%	> 10% upto 50%		
L4-L7	> 10% upto 50%	> 10% upto 50%		
L5-L6	> 10% upto 50%	> 10% upto 50%		
Layer Pair\PCB Design	**PCB Design E**	**PCB Design E BGA**	**PCB Design F**	**PCB Design F BGA**
L1-L8	> 10% upto 50%	> 10% upto 50%	< 10%	> 10% upto 50%
L2-L7	< 10%	> 10% upto 50%	< 10%	< 10%
L3-L6	> 10% upto 50%	> 10% upto 50%	< 10%	< 10%
L4-L5	> 10% upto 50%	> 10% upto 50%	< 10%	< 10%

Layer Pair Balance < 10% Layer Pair Balance > 10% upto 50%

Figure 4. Results of copper balancing density (%) by symmetric layer pairs for designs D, E, and F. The improved layer pairs with less than 10% offset are highlighted in green over red which had offset between 10% and 50%.

Design E, and F were SMT TV of Design D and had a similar PCB layouts. Design E was an unbalanced design with an unbalanced metal density pairing across 3 out of 4-layer pairings of a 10-layer via-any-layer construction whereas Design F was a balanced design by swapping routing and ground layers to balance opposite layer pairs with the same any-layer construction.

PCB Manufacturing

All the thick PCB designs were of the Type 3 category and were laminated using a single lamination process. A 2-up multi-pack panel layout was used to populate a supplier production panel. 4 supplier production panels were stacked together and separated by a separator plate in a compartment also commonly referred to as a book. Towards either end of the book, heating plates serve a dual purpose of heating and pressing the panels together during the press cycle. Multiple book configurations are pressed together during lamination. For this study, a total of 6 books were pressed in a single lamination cycle as shown in Figure 5. A standard lamination process was adopted to heat the panels under pressure in a vacuum to achieve resin flow between multiple copper – prepreg stacks for bonding them together.

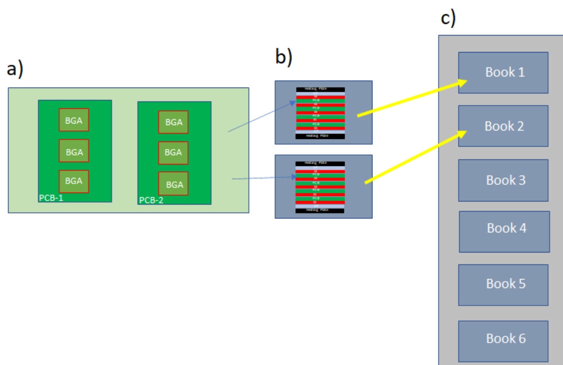

Figure 5. a) Thick PCB 2-up multi-pack supplier production panel b) Book layout used to produce 2-up supplier production panel c) Total book stack in a press system for building PCB designs A, B, C.

Type 4 thin PCB designs go through multiple lamination processes as compared to thick PCB designs. Similar book configurations consisting of multiple supplier production panels as described above were used except a supplier production panel had twelve 2-up multipacks instead of just two. Additionally, 10 supplier production panels were stacked together in a book and subjected to four lamination cycles instead of just one. Adjustment to the thickness of separator plates were made with the advancement of lamination cycles to account for increase stack thickness per lamination cycle. Tracking of the panel location in a book per lamination cycle was maintained. Figure 6 shows a schematic of the multi-pack used and the book structure used to manufacture thin PCB designs. Again, a standard lamination process was adopted to achieve bonding between the stacks to create thin PCB designs D, E, and F.

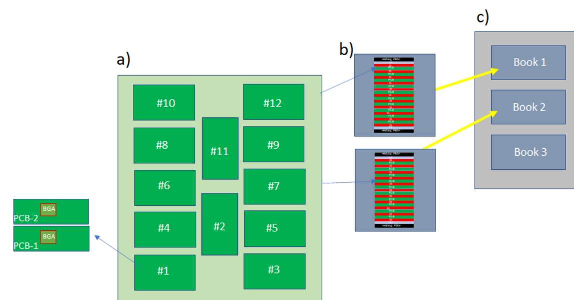

Figure 6. a) Thin PCB twelve 2-up multi-pack supplier production panel b) Book layout used to produce twelve 2-up supplier production panel c) Total number of book stacks in a press system for building PCB designs D, E, F.

PCB BGA LAND PATTERN WARPAGE CHARACTERIZATION AND MANUFACTURING IMPROVEMENTS

It became imperative to understand the impact of PCB manufacturing influence for different PCB TV designs laid out in the earlier section. Manufacturing impact was assessed through mapping of surface deformations in the PCB BGA land pattern post-press lamination cycle. Various surface deformation measurement techniques exist with the fringe-based measurement technique being the most popular in the PCB industry. The fringe-based technique relies on mapping out deformation-through interference fringe patterns formed or projected on the surface and generally requires surfaces to be coated for accurate measurements [7]. A confocal technique instead can map out similar surface deformation with reasonable accuracy without a need to coat the surface. A commercially available optical profilometer with a line sensor capability and submicron level z resolution was utilized for the measurement of incoming PCB BGA land pattern warpage. The warpage was estimated by fitting a regression plane through the measured data points and calculating a difference between the highest and lowest data points. A sign convention adopted was positive for the frowny profile and negative for the smiley profile as shown in Figure 7.

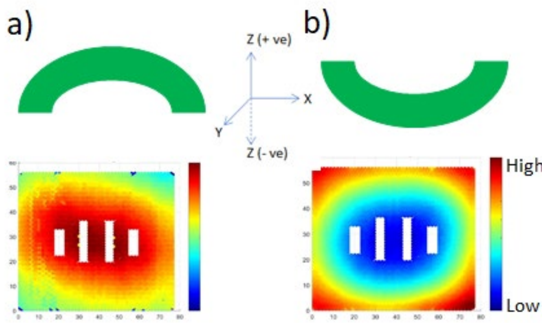

Figure 7. Warpage sign convention adopted for this study a) +ve warpage sign – frowny shape b) -ve warpage sign – smiley shape

Thick PCB Manufacturing Influence

To rule out any impact from the shipment process of PCBs from source to destination, incoming room temperature warpage measurements were done at both source and destination sites. Measurement results from both sites were in good agreement showing similar PCB BGA land pattern warpage variation with a mean difference of less than 5um as shown in Figure 8. The source of this mean difference could be attributed to different measurement techniques used between sites for measuring PCB BGA land pattern warpage. For each PCB design, a detailed log of traceability was maintained for the working panel, multipack panel, and individual PCB in a multipack panel as they went through different manufacturing lamination process steps as described in section 2.

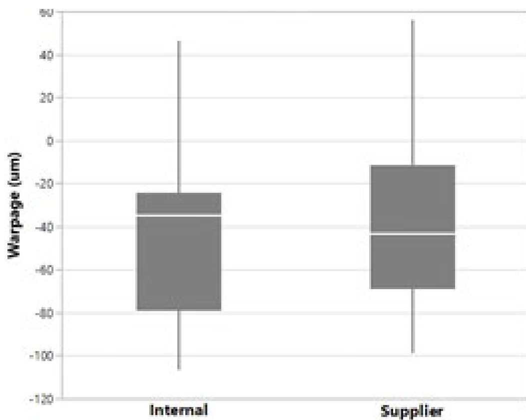

Figure 8. Incoming PCB BGA land pattern warpage variation between supplier and internal site.

Thick PCB TVs with designs A and B showed high incoming PCB BGA region warpage variation as shown in Figure 9. Further analysis of the PCB design A warpage data showed a specific warpage trend. This trend aligned with panel location in a book for a typical press lamination recipe comprised of 4 panels per book as described in section 2. PCB BGA land pattern warpage at book location 1 showed a smiley PCB BGA land pattern warpage whereas that at book location 4 showed a frowny PCB BGA land pattern warpage. Locations 2 and 3 had PCB BGA land pattern warpage in the middle and were less smiley as shown in Figure 10. Localized deformation profiles of the top and bottom surface of the PCB BGA land pattern region showed an opposite deformation pattern for panel locations 1 and 4 of a book as shown in Figure 11. Book location 1 showed top surface deformation rendering it to go more smiley whereas book location 4 showed bottom surface deformation making it to go slightly frowny on the top surface. These localized deformations, also referred to as embossing, are indicative of the flow of prepreg material resulting from core deformation due to sparse copper distribution across the z-stack of the BGA land pattern.

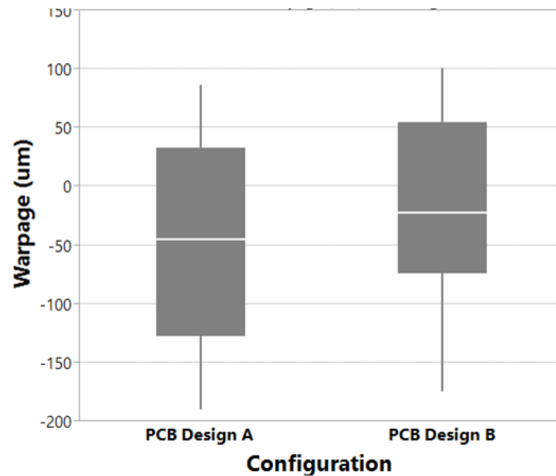

Figure 9. Manufacturing variation observed between different PCB designs.

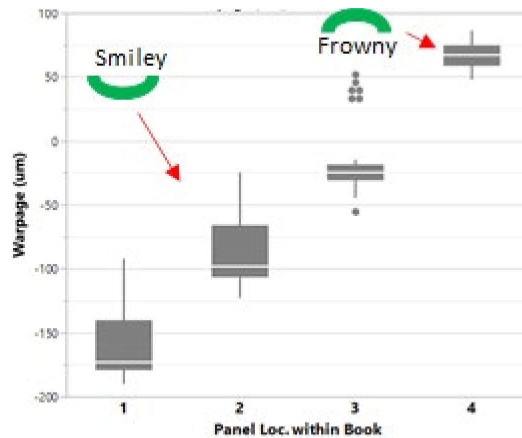

Figure 10. Source of incoming PCB warpage variation traced to location of panels within a book configuration.

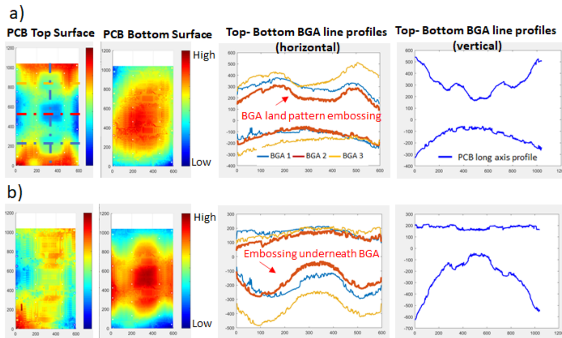

Figure 11. PCB surface deformation maps along with BGA land pattern line scans in a horizontal direction across 3 BGA locations and vertical direction across the center of PCB: a) PCB at book location #1 b) PCB at book location #4; red arrow shows BGA land pattern embossing

To understand the impact of copper balance, PCB design C, a variant of the PCB design A design with an improved layer pair balancing scheme, was manufactured under the same process condition. Figure 12 shows PCB BGA area warpage with lower variation for Design C as compared to Design A, highlighting the impact of copper imbalance on warpage during the manufacturing process

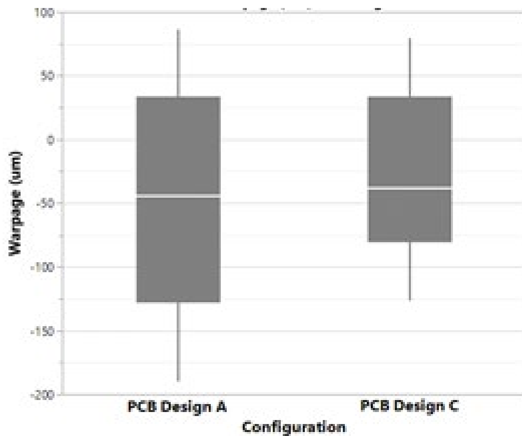

Figure 12. Influence of PCB design on incoming PCB BGA land pattern warpage variation

Thick PCB Manufacturing Improvements

PCB design B had a better layer pair balancing scheme as compared to PCB design A but continued to show high warpage variation. To trace the source of this variation, changes were made to the PCB lamination book lagging structure and compared with the POR structure. Incoming PCB BGA land pattern warpage was measured, and it was observed that alterations of lamination book structures helped to reduce the PCB BGA land pattern warpage variation as shown in Figure 13. This highlights the manufacturing process as an additional source of warpage variation.

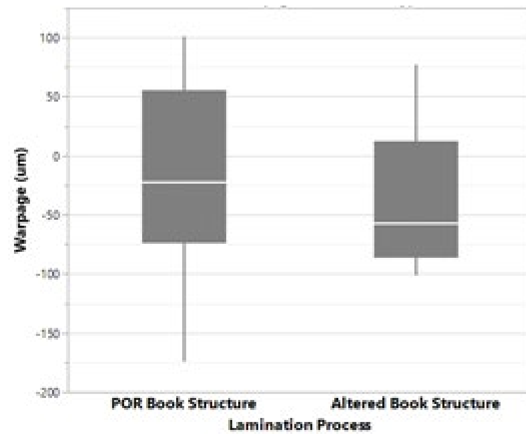

Figure 13. Influence of PCB manufacturing recipe on incoming PCB BGA land pattern warpage variation.

In addition to the lamination structure changes, separate alterations were made to the PCB design A stack by selecting a POR prepreg material stack comprised of just low loss prepreg material. This was compared with an Altered prepreg material stack, where a combination of a low loss and a standard prepreg material was used. A low loss core material was used on both these stacks. Table 2 shows the differences in material stacks for a 22-layer PCB design A stack.

Table 2. PCB design A layer stack with prepreg material changes

Layers	POR Prepreg Material	Altered Prepreg Material
L1-L2, L3-L4, L5-L6, L7-L8	Low Loss	Low Loss
L9-L10	Low Loss	Standard
L11-L12	Low Loss	Standard
L13-L14	Low Loss	Standard
L15-L16, L17-L18, L19-20, L21-L22	Low Loss	Low Loss

It was observed that the PCB BGA land pattern warpage variation was greatly reduced through a choice of the right prepreg material as shown in Figure 14. This was due to better flow ability of standard prepreg material over a low loss material leading to reduced core deformation. This highlights the need to carefully select materials as they can act as an additional source of warpage variation. The dynamic PCB warpage of the thick PCB designs A, B & C was stable across the SMT assembly temperature, and hence focus was shifted on understanding the incoming PCB BGA region warpage and its correlation to SMT defects as discussed in the following section.

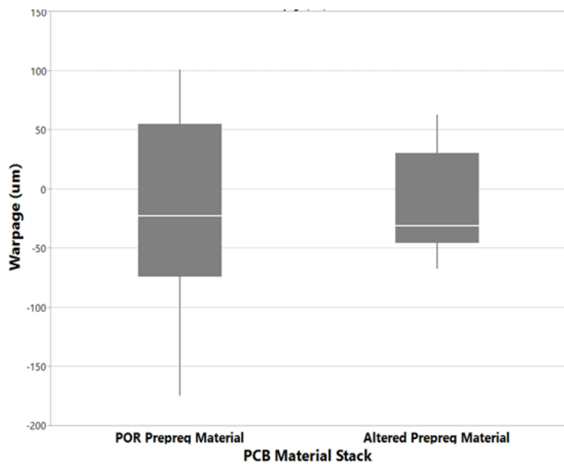

Figure 14. Influence of PCB material stack on incoming PCB BGA land pattern warpage variation.

Thin PCB Manufacturing Influence & improvements

A similar approach of characterizing incoming PCB BGA land pattern warpage was also adopted on thin PCB designs. Thin PCB designs had 12 multipacks per working panel. Working panels from top, middle and bottom locations of the book were selected to understand warpage variation across the book. Warpage was measured on all the multipack location on these working panels to understand spatial location impact. PCB design D was specifically chosen to for this purpose to understand Type 4 manufacturing process influence on PCB BGA land pattern warpage. The BGA footprint was smaller, and it had a smaller warpage magnitude with smiley shapes. The PCB BGA land pattern warpage trend obtained for the panel locations within a book had similar warpage variation for each location as shown in Figure 15. To understand the source of the outliers at some panel locations, warpage variation for each multipack location on a working panel was compared as shown in Figure 16. It was observed that multipack panels that were close to the edge of the working panel showed more outliers in comparison to those in the center.

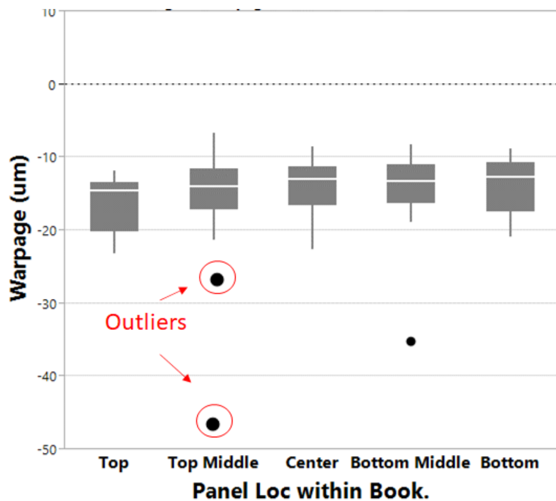

Figure 15. Incoming thin PCB warpage variation based on the location of the panels within a book configuration.

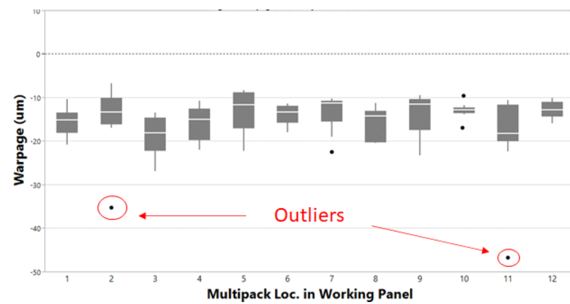

Figure 16. Incoming thin PCB warpage variation based on multi-pack location within a working panel.

To understand the impact of copper imbalance, thin balanced PCB design F warpage results were compared with unbalanced PCB design E. Balanced PCB design F showed less PCB BGA land pattern warpage variation than an unbalanced PCB design E as shown in Figure 17. Additionally, different shape distributions were observed between the balanced design F and an unbalanced design E where unbalanced design E smiley warpage shape was more in line with increasing direction of layer pair imbalance.

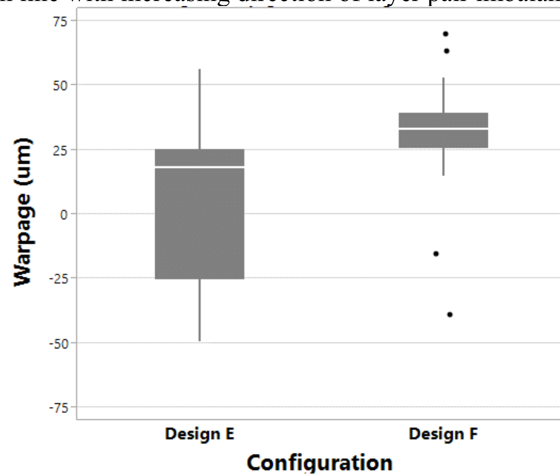

Figure 17. Influence of thin PCB design on incoming PCB BGA land pattern warpage variation.

In general, it was observed that the manufacturing process induced warpage variation was small for Type 4 PCBs manufactured using a multi-lamination cycle. As a result, further modifications to the book structure or prepreg materials were not considered on thin PCB designs.

SMT YIELD ASSESSMENT

SMT experiments on thick and thin PCBs were carried out using two different BGA packages. Details of BGA package types used for the yield study are shown in Table 3. The SMT process followed a standard flow with solder paste printing, solder paste inspection, component placement, and reflow. The reflow process used a near eutectic low temperature reflow profile with a 165°C to 175°C peak reflow temperature. PCBs were supported in a pallet during SMT to minimize the sag of PCBs during SMT. Post SMT, all assembled PCBs underwent automated X-ray inspection and destructive failure analysis such as cross-section (XS) and dye and pry (DNP).

Table 3. BGA package details used for SMT study

Parameter	Large BGA Pkg	Small BGA Pkg
BGA X, Y, Z dimensions	77.5mm x 62.5mm x 5mm	23mm x 19mm x 2mm
BGA Pitch	1 mm	0.5 mm
BGA Ball Diameter	0.610 mm	0.250 mm
Solder Ball Metallurgy	Near Eutectic Sn-Bi	Near Eutectic Sn-Bi
Solder Paste Metallurgy	Eutectic Sn-Bi	Eutectic Sn-Bi

The developed SMT process was held constant to reduce process variation and resulting impacts on the SMT yield and solder joint height (SJH). The BGA package dynamic warpage through SMT reflow was smiley (-ve) in shape with insignificant warpage magnitude levels and package-to-package variation. Similarly, the PCB dynamic warpage through SMT reflow was also found to have minimal warpage change in comparison to the incoming room temperature PCB BGA land pattern warpage. As a result, the package warpage and PCB dynamic warpage were insignificant factors regarding SMT yield and SJH assessment.

Thick PCB SMT Yields

The incoming PCB BGA land pattern warpage values for BGA locations were correlated to individual PCB serial numbers and were used to selectively assess SMT yields. PCBs at the tail end of warpage distribution with differing shapes for each of the PCB designs were selected for SMT. PCBs used for assessment were tracked through the SMT and failure analysis steps. Final yield values and SJH were correlated to the room temperature PCB BGA land pattern warpage.

Table 4. SMT yield based on room temperature PCB BGA land pattern warpage shape.

Parameter	PCB Warpage Shape	PCB Warpage Magnitude (microns)	SMT Yield (%)
PCB Design A	Frowny, +ve	100 and lower	100
PCB Design A	Smiley, -ve	150 and greater	16
PCB Design A	Smiley, -ve	150 and lower	100
PCB Design C	Frowny, +ve	100 and lower	100
PCB Design C	Smiley, -ve	100 and lower	100

PCB design A with smiley warpage greater than 150 microns showed SMT defects whereas all the other cases showed no yield loss as shown in Table 4. All defects occurred at the package corners where the smiley PCB BGA land pattern warpage combined with the package warpage resulted in the most significant solder joint compression. Figure 18 shows the mechanism for the occurrence of solder bridging defects at BGA package corners.

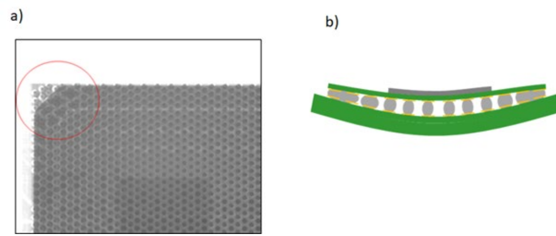

Figure 18. a) SMT solder bridging defect b) incoming PCB concave warpage causing solder bridging defect at the corner of BGA package.

Figure 19 depicts the SJH across the same row of three different BGA packages that were soldered onto PCBs with PCB land pattern warpages of smiley - 180 microns, frowny - 150 microns and smiley - 20 microns. The SJH was measured from the top of the PCB pad to the bottom of the substrate pad and was collected for each solder joint across the XS row. Measured SJH profile shapes are opposite to the PCB BGA land pattern warpage shape indicating a higher contribution from PCB incoming warpage for the same BGA package warpage shape, smiley in this case.

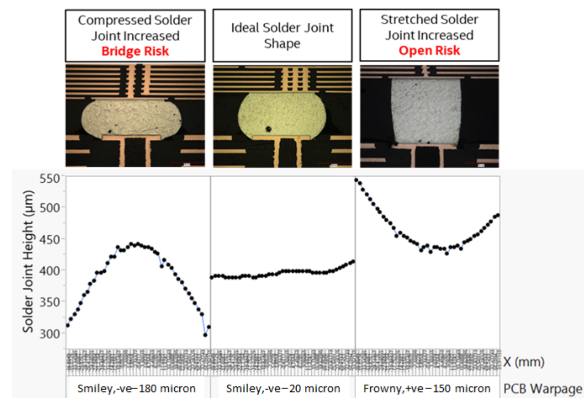

Figure 19. Solder joint height profiles for 3 different incoming PCB BGA land pattern warpage levels

Thin PCB SMT Yields

Preliminary SMT results show no SMT defects for a balanced PCB design F with tight warpage magnitude and shape variation. Data collection is still in progress on an unbalanced PCB design E with high variation in magnitude and shape. Thin PCB SMT results, and recommendations will be shared in next year's technical publication.

DESIGN AND MANUFACTURING RECOMMENDATIONS

Design Recommendations

The physical design and PCB architecture should be balanced to mitigate warpage risk during lamination and fabrication. The importance of opposing layer assignment similarity enables a balanced construction. Opposing layers assigned as signals typically result in lower copper density. Assigning opposing signal layer assignments will enable balanced

designs as would the assignment of higher copper density power and ground layers. Targeting a maximum percentage delta such as 10% allows for some design flexibility while minimizing warpage risk.

The within-layer metal density balance and uniformity should equally be considered at the design stage. Local accumulation of high-density delta regions may present low-pressure zones resulting in surface embossing or local coplanarity differences. Further characterization of local press thicknesses and resulting coplanarity may be required if the design is not balanced. Various methods of balancing local copper have been demonstrated such as optimizing metal fill, utilizing pad suppression, and optimizing connectivity to achieve within-plane balanced designs.
Design tools have demonstrated metal usage report capabilities of specific features and various characterization methods that should be utilized to evaluate copper density balance. In addition, the outer panel frame should be utilized to balance the design.

Material Recommendations
Making the right choice of a prepreg material is important from an electrical and thermal standpoint. Low loss prepreg materials are widely used in high-speed signal transmission applications due to better electrical characteristics. However, flow ability of a low loss prepreg material is marginal and often requires a special lamination press profile with high temperatures and pressures. Standard prepreg material behavior is different, creating a need to tailor a hybrid material stack to get desired performance benefits. Careful consideration needs to be given while choosing a hybrid material stack comprised of both a low loss and a standard prepreg material. It's recommended to use standard prepreg material in the center to get better flow and less core deformation and restrict the use of low loss prepreg materials to the periphery to get electrical benefits.

Manufacturing Recommendations
The PCB lamination process step during PCB manufacturing is the biggest source of PCB warpage variation as shown with a balanced PCB design warpage cases in earlier sections. Lamination recipe modification discussed in this study is effective in reducing PCB warpage variation however optimization of the lamination recipe is recommended during the early stages of the lamination cycle development for any custom PCB designs. Studying PCB surface deformation during lamination recipe development is valuable in building an understanding of influential lamination process knobs. PCB surface deformation effects can be subdued through proper choice of book configuration, proper material selection along with adjustments to localized copper distribution in the PCB BGA land pattern region. Hence equal attention needs to be given to the material selection and design as well during lamination recipe development. In cases where recipe optimization limitations exist, appropriate dummy structures can be introduced in a press book configuration to reduce the PCB BGA land pattern warpage variation.

Some of the above-discussed solutions can help in minimizing incoming PCB BGA land pattern warpage variation where complex routing requirements governed by architecture/electrical demands make it difficult to drive design for excellence (DFX) changes.

SUMMARY
As technology continues to scale, understanding and controlling PCB BGA land pattern warpage is critical to achieve high SMT yields. Findings from this work have highlighted 3 vectors namely PCB copper layer pair balance, PCB material selection, and PCB lamination process optimization as the key knobs to minimize and control PCB BGA land pattern warpage. Below are the summarized recommendations.

Control PCB layer pair copper density balancing to less than 10% as a design parameter to better balance PCB designs. Both thick and thin PCBs manufactured using single and multi-lamination processes have shown to benefit from this design recommendation in keeping warpage variability under control. Balanced PCB designs show less variation in incoming PCB BGA land pattern warpage. Additionally, the methodology adopted for SMT cliff assessment at different warpage levels has shown to quickly highlight any SMT issues due to excessive PCB BGA land pattern warpage.

Proper PCB material selection has aided in meeting electrical requirements at low warpage levels. Thick PCBs with specific high-speed requirements have benefited from a hybrid material stack construction. Better flow ability of a standard prepreg material during lamination process is shown to aid in reducing PCB BGA land pattern warpage on a hybrid material stack

The lamination process has the biggest impact on the PCB BGA land pattern warpage. Thick PCB designs (Type 3) manufactured using a single lamination process show high warpage variability mainly due to the configuration within a book structure. Book lagging structure adjustments in conjunction with surface deformation characterization offer benefits in developing an optimized lamination process recipe for better warpage control. Thin PCB designs (Type 4) subjected to a multi-lamination process show comparatively less sensitivity to a book structure.

ACKNOWLEDGEMENTS
Authors would like to acknowledge contributions of Chris Alvarez, Dungh Nguyen, Donald Coburn, Abhishek Das and Type3, Type 4 PCB suppliers for their help in supporting this study.

REFERENCES
[1] Rao.R.Tumala, “Fundamentals of Microsystems Packaging”, McGraw-Hill Publication, 2001.
[2] R Lasky et al., “Principles of Electronic Packaging”, McGraw-Hill Publication, 1989.
[3] R.H. Clark, “Handbook of Printed Circuit Manufacturing”, Van Nostrand Reinhold, 1985.
[5] J. Zundel, T. Krivec, Q. Tao, M. Frewein, S. Stojanovic, “Panel level warpage simulation of PCB comprising electrical components”, *21st International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, 2020, pp.1-7.*
[6] T. Amla, “Predicting dimensional deformation during lamination for multilayer PCB”, Isola, 2008
[7] S. Aravamudhan, C Combs, A. Prasad, A Abraham, “Multifaceted approach to minimize PCB warpage in Board assembly process”, *SMTAI Conference Proceedings,* Sept 25-29, 2016, pp. 168-176.
8] S. Walwadkar, T. Harris, B. Zhou, A. Vaidya, J. Landeros, A. McAllister, “Influence of PCB surface features on BGA Assembly Yield” *SMTAI Conference Proceedings,* Sept 25-29, 2016, pp. 375-582.