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Functional System Observations of Tin-Bismuth Low Temperature Solder Electromigration Behavior

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ABSTRACT
The growing use of tin-bismuth (SnBi) based low temperature solder (LTS) in the electronics industry is driving increased research into how these metallurgies differ in behavior compared with Tin-Silver-Copper (SAC) solders. One area of interest is electromigration (EM). EM at the second-level interconnect (SLI) has not been a primary focus area for SAC-based systems. Bi, however, has higher mobility with current flow and thus understanding the risk for EM is valuable. There is a need to understand how electromigration may occur in systems and how best to select acceleration conditions to reduce time to data when assessing design risk. Significant work has been completed recently studying electromigration behavior in LTS-based assemblies using highly accelerated current density and ambient temperature conditions. Given the relatively short history of LTS use for computers, very little data exists to document solder joint microstructure from functional systems with a known usage history. As a result, demonstrating that solder joint conditions post-acceleration meaningfully replicate actual solder joint conditions in the lifetime of interest is challenging. This paper will review a selection of previous results reported from accelerated testing. The results will be compared with cross-sectional results from components on functional systems with known time in service and current density/ambient conditions. Finally, additional areas for research will be noted and suggestions for design related methods for managing electromigration during system design will be proposed.

Key words: Solder, LTS, electromigration, reliability, design, current density, tin, bismuth.

INTRODUCTION
Electromigration (EM) is the phenomenon of forced atomic diffusion resulting from metal atoms being transported due to a driving force produced by an electric field and the resulting electric current in a conductor [1]. First noted in molten tin-lead in 1861 [2], the process remained primarily of academic interest until the development of integrated circuits (ICs). In the late 1960's EM was determined to be the root cause of early life failures in aluminum connections in thin film ICs [2]. As the behavior became a practical issue limiting progress in packaged ICs, research accelerated and has become significantly more critical as semiconductor dimensions reduced from micron to the nanometer scale and the resulting current densities become much larger.

For first level interconnect (FLI) solder joints, EM has been considered a risk for tin-copper (SnCu) and tin-silver-copper (SAC) solder joints given current densities can exceed 1 x 10^4 A/cm^2 [3] However, for the second level interconnect (SLI) solder joints that join the component to the printed circuit board (PCB), the dimensions have been sufficiently large that the resulting current densities did not create a substantial EM risk in those solder systems.

During the lead-free (Pb-free) transition significant work was done exploring the EM behavior differences between tin-lead (SnPB) and the candidate Pb-free solder systems. Eutectic SnBi was a leading candidate to replace SnPb solders and was studied extensively for EM performance. However, once SAC became the industry standard Pb-free choice, industry interest in SnBi declined and less work was done to understand the critical elements necessary to quantify and manage EM in SnBi systems.

Recently, increasing challenges with component and PCB warpage in thin notebook systems coupled with increasing pressure to reduce greenhouse gas emissions has renewed interest in the SnBi system as a lower temperature alternative to SAC [4]. Since the Pb-free transition was completed, component dimensions on notebook motherboards have continued to decrease which increases solder joint current densities. As well, reduced volume chassis designs have had the potential to increase ambient and solder joint temperatures further increasing EM risk.

A growing body of recent work has been published exploring EM related issues for SnBi-based solders. As with any reliability behavior, risk time scales can be long and accelerating behavior to reduce time to data is attractive. Due to the lower melting point of SnBi solders, selection of acceleration conditions for EM research can be challenging. Recent results have been reported with current densities from 500 A/cm2 to 15 kA/cm2 and ambient temperatures from 75C to 125C [5,6,7,8]. One challenge for selecting acceleration conditions is understanding what solder joint conditions at end of life the accelerated results should produce to ensure that observed behaviors are not anomalous [2]. This paper will review common acceleration approaches for EM research as well as factors that can meaningfully modify EM behavior. The paper then reviews solder joint inspection results from several SnBi-based LTS notebook systems with known usage histories. These results can provide a basis for comparison when assessing accelerated

EM results. Additional areas of study and suggested design mitigation approaches will be proposed.

ELECTROMIGRATION RISK ASSESSMENT

Acceleration Condition Considerations

In a 1969 paper, James Black of Motorola reviewed the status of electromigration research and proposed an equation to describe the behavior [9]. The equation (1) proposes that mean time to failure (MTF) is inversely proportional to the square of the current density and has an exponential dependance on temperature.

$$\frac{1}{MTF} = AJ2e - \varphi/kT \qquad \text{Equation 1}$$

Where:

MTF = mean time to failure (hr)
A = material constant related to cross-sectional area
J = current density (A/cm^2)
ϕ = activation energy (eV)
k = Boltzman's constant
T = temperature (K)

The choice of test temperature to use for acceleration should be made with an understanding of the resulting homologous temperature (Th) for the solder system being evaluated. Tm is the ratio of ambient temperature to the material melting temperature. Table 1 summarizes the Th for SAC and eutectic SnBi solders at several common acceleration ambient temperatures.

Table 1. Homologous temperature comparison of SAC and Sn58Bi solders

Homologous Temperature (Th)		Ambient Temperature (˚C)		
Solder Material	Melting Temperature (˚C)	75	100	125
SnAgCu (SAC)	217	0.35	0.46	0.58
Sn58Bi	138	0.54	0.72	0.91

Ho and Thomas [2] have noted that at moderate temperatures lattice diffusion in the material bulk is significantly less than at the grain boundaries. If the chosen acceleration ambient is significantly above a Th of 0.5 but the expected operating conditions are at or below a Tm of 0.5, the failure mechanisms in acceleration may not match the expected operational failure mechanisms.

With the strong influence of current density on SnBi EM behavior, investigators often select current densities well above those expected to be experienced in an actual system design. Careful attention must be paid to the potential increase in solder joint temperature due to current induced joule heating. Selecting an ambient temperature that, with the addition of joule heating at the chosen current density, results in an overall solder joint temperature that approximates the expected Th should allow electromigration behavior to be accelerated using higher current density without introducing non-representative artifacts.

Process Inputs

Eutectic SnBi has been the basis for a significant amount of EM research. The eutectic composition eliminates the need to account for the role any dopant additions might play in the EM results. As well, eutectic SnBi solder pastes are readily available from most major solder paste vendors which simplifies paste sourcing and ensures that results can be compared across studies using different paste vendors.

Comparing the EM behavior of SAC and eutectic SnBi solder joints at 100 C (Th = 0.72) and 2.08 kA/cm2, Xu et. al. [10] reported that while the homogenous SnBi solder joint IMC was approximately half the thickness of the SAC solder joint at time 0 (T0), after 500 hr of stressing, the SnBi IMC was significantly thicker than the SAC control samples. As well, the vacancy exchange with the Bi resulted in large voids forming at the cathode side of the joint. At an ambient temperature of 75 C (Th = 0.54) and a current density of 5.0 kA/cm2, Shafiq and Chan [8] report that the eutectic SnBi samples showed significant grain coarsening and a continuous layer of Bi formed at the anode side. These results illustrate that while eutectic SnBi is an attractive research tool, the behaviors are non-ideal for practical applications.

A great deal of work has been published evaluating the potential for dopant additions to improve the EM performance of SnBi LTS solders. Ag has been shown to provide meaningful improvement in EM resistance [6,8,11] with the proposed mechanism being small Ag3Sn inclusions inhibiting the Bi migration. For example, Shafig and Chan [8] demonstrated that with 2% Ag addition to eutectic SnBi, the SnBiAg samples showed much finer grain structure and no apparent Bi accumulation after 480 hr of current stressing at 5.0 kA/cm2. Antimony (Sb) and Nickel (Ni) have also been found to improve EM behavior in SnBi solder joints [11,12]. Due to the beneficial effects of dopants on EM performance as well as the mechanical capabilities of SnBi solders [13,14], there are an increasing number of highly engineered SnBi LTS products being introduced to the market. These doped LTS products are finding adoption as manufacturers select solder products for their SnBi-based manufacturing.

Solder joint Bi concentration is another factor that must be considered when assessing EM risk. As previously noted, much of the EM literature is based on eutectic SnBi solder joints with 58% Bi. The relatively high concentration of Bi in the SnBi solder joint has been shown to result in rapid accumulation of Bi at the anode at 75 C (Th = 0.54) and 5.0 kA/cm2. In a flip chip study of Cu pillars assembled with either Sn58Bi or Sn30Bi, resistance change at 3000 hr of current stressing for Sn58Bi was 65% while the Sn30Bi samples had a 20% change in resistance [15]. A note of

caution must be made when considering the reduction of Bi % as an EM risk mitigation strategy. For components with a risk of T0 hot tearing, the strongest variable for eliminating the hot tear behavior is reducing reflow peak temperature [16]. With reduced Bi %, the amount of reflow peak temperature reduction will be limited vs. eutectic SnBi and may raise the risk of hot tear impact for certain components.

Solder joint construction can also play a role in EM performance of SnBi-based solder joints. In a homogenous SnBi solder joint, EM induced Bi accumulation occurs at the anode at approximately the same rate regardless of the current direction. However, Hadian, Genanu, and Cotts [6] documented a more complex EM behavior for hybrid SAC305-SnBiAg solder joints. For current flow towards the hybrid region, a typical EM signature of Bi accumulation at the anode was observed. However, due to the Bi concentration gradient, Bi diffusion was also noted towards the cathode. For current flow from the hybrid region through the un-melted SAC portion of the joint, moving Bi across the SAC portion of the joint required an order of magnitude greater time to reach the anode. For Sn58Bi, Xu, Cai, and Pham [10] noted significant Bi accumulation and void formation/solder joint failure in homogenous SnBi samples while the SAC and hybrid SAC-Sn58Bi samples did not exhibit Bi accumulation after the 480 hr stress period at 2.08 kA/cm2 and 100 C ambient.

Component and PCB surface finish is an additional variable that contributes to the EM performance of SnBi based solders. Electroless Nickel-Immersion Gold (ENIG) finishes have been shown to have lower mechanical performance for both SnBi and SAC based solder joints compared with Copper Organic Surface Protectant (Cu-OSP) finishes [14,17]. Electroless Nickel-Electroless Palladium-Immersion Gold (ENEPIG) is a common component pad finish and is finding increased use as a PCB pad finish in some market segments. Kim, Lee, et. al. [18] found that for Sn58Bi solder joints current stressed at 13.0 kA/cm2 at 100 C ambient, mean time to failure for samples assembled on Cu-OSP was 6372 mins compared to 5284 mins for ENEPIG and 4568 mins for ENIG. While it can often be difficult to select component pad finishes, designers have more freedom on the selection of PCB surface finish and it should be a consideration when designing for EM performance.

FUNCTIONAL SYSTEM ELECTROMIGRATION

System Design Considerations

For notebook and desktop systems, the changes in work practices due to the pandemic have resulted in significant modifications to use case assumptions used as part of the system design process [19]. Historically, a significant portion of the workday was spent with in-person meetings where system use intensity was low. The move to remote work resulted in the workday involving many hours of contiguous video meetings where system use intensity was relatively high. The new use model creates the potential for higher sustained motherboard temperatures and longer periods of the central processing unit (CPU) running at the maximum design steady-state current density. These changes make it particularly important to understand the behavior of actual component solder joints in both accelerated and use case situations in order to make informed design choices.

Power delivery networks (PDN) are generally designed with three main components. The CPU, a power inductor, and a power field effect transistor (FET) make up an individual power delivery phase. To manage mother board temperatures and current loads, a particular voltage rail may be divided into multiple phases with several inductor/FET pairs feeding the CPU rail. The current density for a given component can be determined by calculating the total component pad area and then dividing it by the expected current load per phase.

A functional LTS based motherboard was used to understand EM behavior in production solder joints with accelerated thermal and current density inputs. The motherboard used an ENIG surface finish and was assembled with a Sn50Bi + Cu solder paste. The test approach was designed to allow the CPU to be held at the maximum allowed current. Under normal operating conditions, reaching this level of current would only be sustainable for micro-seconds before the CPU would throttle. Assuming the maximum allowed current load, the current density was calculated for each of the key PDN components (Table 2). The power FET is the PDN component with the highest current density.

Table 2. Calculated current density for components under test

Component	Current Density (A/cm2)
Power FET	3.11E+03
CPU/pin	6.12E+02
Power inductor	3.70E+02

The motherboard was tested outside of the chassis and external blocks were used to restrict airflow and increase the solder joint temperatures. Temperatures were measured using an IR thermometer. Due to the power FET being a bottom terminated component, it was not possible to directly measure the solder joint temperatures. As a proxy, temperatures were measured at the power inductor solder joints adjacent to the power FET. Temperatures were monitored for three motherboard phases. The target solder joint temperature was 85 ˚C. If the temperature exceeded 90 ˚C, the current load would be reduced to return the temperature to the target solder joint temperature.

T0 input current produced a calculated power FET current density of 3.04E+03 A/cm2 and an average inductor solder joint temperature of 87.4 ˚C. After 214 hours of continuous current stressing, average solder joint temperatures reached 97.8 ˚C. The current load was reduced to 2.33E+03 A/cm2 and at 217 hours the average solder joint temperature was 88.3 ˚C. However, by 223 hours the solder joint temperatures had reached an average of 96 ˚C which was followed shortly

by open circuits on two of the phases. Table 3 details the current density and solder joint temperature readings.

Table 3. Current density and solder joint temperature vs. test time

		Average Solder Joint Temperature ('C)		
Time (hr)	Power FET current density (A/cm2)	Phase 1	Phase 2	Phase 3
0	3.04E+03	85.7	86.3	90.3
172.5	3.04E+03	87.6	89.1	89.3
214	3.04E+03	97.1	97.7	98.6
217	2.33E+03	88.8	88.1	87.9
223	2.33E+03	96.2	96.7	95.1

Power FETs and inductors were then cross-sectioned (XS) to compare solder joint conditions of as-reflowed samples with post-current stress samples. At T0, PCB side IMC thickness for both component types ranged from 0.18um to 0.5um. The very thin IMC can be attributed to the ENIG PCB surface finish. Both components had Sn pad finish and resulting component side IMC thickness ranged from 0.9um to 2.8um. Figure 1 shows T0 solder joint condition for the power FET and Figure 2 illustrates the power inductor. Both components showed a typical SnBi lamellar structure.

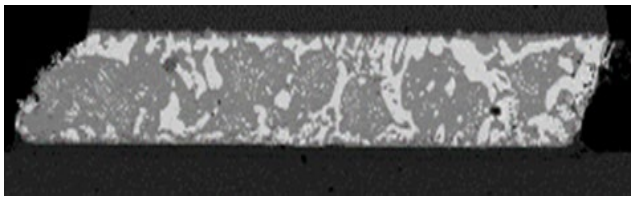

Figure 1. T0 power FET solder joint microstructure

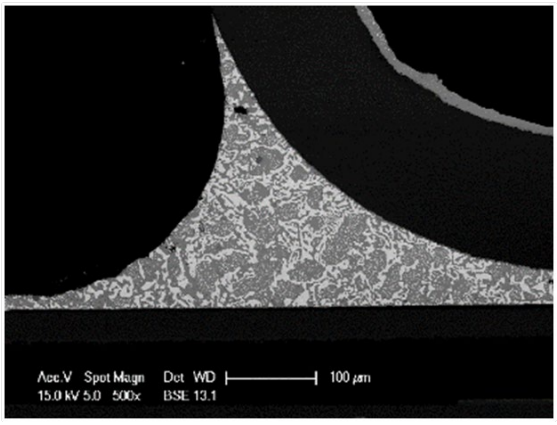

Figure 2. T0 power inductor solder joint microstructure

For post-test samples, the power inductors showed a coarsened grain structure which would be expected after an extended period above 85 ˚C. PCB side IMC thickness had increased to 1.2 um to 2.2 um. Component side IMC thickness had increased less significantly to 2.0 um to 3.2 um. Given the lower current density, no signature of Bi EM was noted (Figure 3).

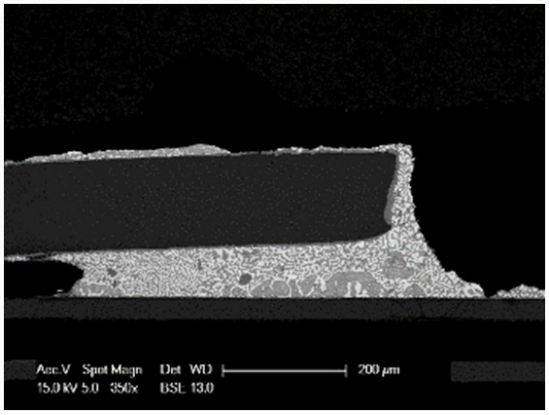

Figure 3. Post-current stress power inductor solder joint microstructure

The post-stress power FET solder joints also showed phase coarsening typical of extended time at high temperatures. While Bi migration was clearly visible in many samples (Figure 4), the primary cause of open solder joints appears to be rapid IMC growth that consumes the constituent metal leaving large, contiguous voids. While a continuous layer of Bi would be expected to prevent IMC growth, localized melting due to resistance increase of the Bi layer would allow Sn sufficient mobility to drive continued IMC growth [20]. In several cases, IMC growth extends into the Cu PCB pad (Figure 5).

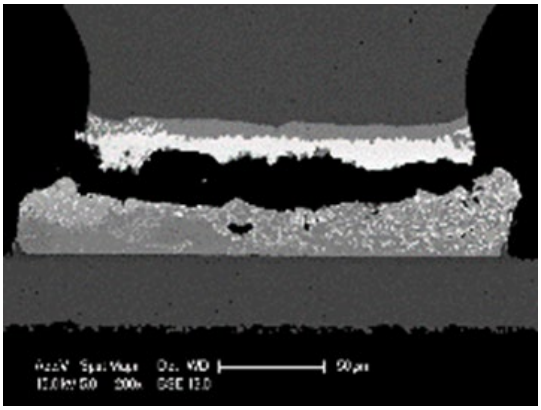

Figure 4. Post-stress power FET solder joint showing EM driven Bi accumulation

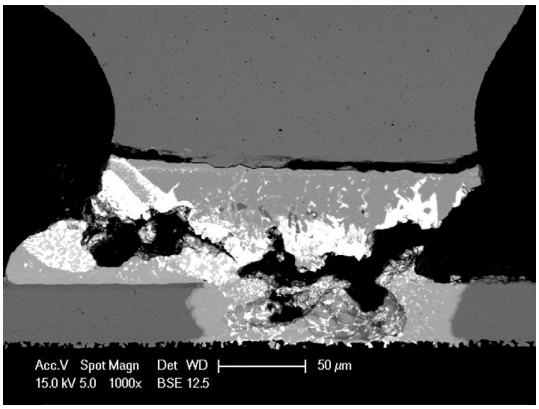

Figure 5. Post-stress power FET solder joint showing excessive IMC growth without continuous Bi accumulation.

Reviewing the post-stress solder joint condition results, effects of current stressing on the power FET components are comparable to many of the results reported in the literature. Comparing the microstructure for the power inductor and FET, it is believed that the actual solder joints temperatures for the power FET were significantly higher than the inductor and would account for rapid IMC growth. These results help understand the solder joint microstructure evolution and possible failure mechanisms in high-risk motherboard components. However, if actual solder joint temperatures were significantly above a Th of 0.5, the failure behavior may not be a reliable predictor of actual s
older joint performance.

Functional System Post-Service Solder Joint Conditions

To compare the solder joint condition of an LTS-based notebook system after extended use with the results obtained with accelerated testing, two notebook systems that had been in active corporate daily use for approximately 2.5 years were obtained. In addition, an unused system of the same model was XS to provide a comparison to the as-built condition. Individual component suppliers were different than the board used for accelerated testing, though the design approach was comparable. For the power rail of highest current load, the use condition boards used a three-phase design with PDNs comprised of power FET and inductor pairs supplying the CPU (Figure 6).

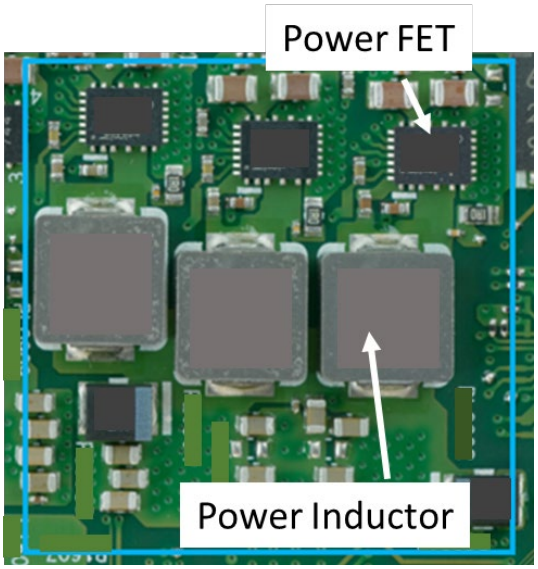

Figure 6. Three phase PDN design evaluated for use condition notebook systems

The boards are believed to be assembled with a 30-40% Bi solder paste that contains less than 1% addition of Cu. Based on the maximum sustainable current load for the power FET, per pin current density was calculated to be 1.64E+03 A/cm2. Solder joint temperatures during operation are not known, however modeled motherboard temperatures adjacent to the CPU at maximum sustained current load are approximately 70 ˚C and the system design includes a fan for thermal management.

The as-built system had been stored at approximately 25 ˚C for two years with no bias. Evaluating the solder microstructure at a power FET pin, typical larger islands of Bi are present. The extent of the Bi regions appears consistent with a lower Bi % paste. Some voiding is also present which is typical for these components. The PCB surface finish is Cu-OSP and IMC thickness was measured at 1.9 to 2.2um (Figure 7).

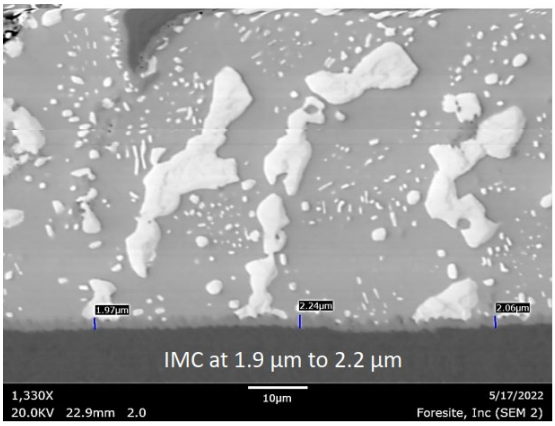

Figure 7. As built power FET solder joint microstructure, 2 years of room temperature storage with no bias

Comparing the as-built FET solder joint condition to the 2.5 year operational life System A, the solder joint condition appears little evolved. Figure 8 shows the overall solder joint condition for a FET switch pin while Figure 9 provides a higher magnification view of the microstructure. Little change from as built is apparent with no evidence of Bi migration or significant IMC growth. IMC thickness was measured at 1.5 to 2.5 um.

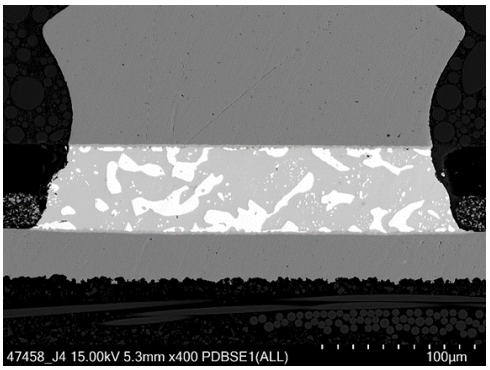

Figure 8. System A, power FET switch pin post-2.5 years daily corporate use

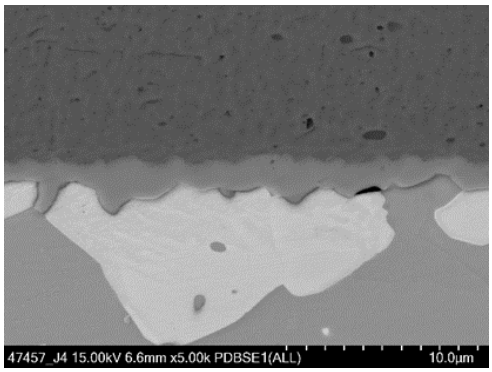

Figure 9. System A, 5000X view of power FET solder joint microstructure

System B provided a contrast with System A. Solder joint condition in System B appears similar to what would be expected with a T0 solder joint. There is no evidence of Bi migration or excessive IMC growth in this example. Figure 10 provides a full view of the power FET switch pin, while Figure 11 illustrates a higher magnification view of the solder joint microstructure. However, the System B microstructure appears to represent a higher Bi % solder paste. Compositional analysis (Table 4) provides support for this conclusion. The as-built system has roughly twice the Bi as the System B solder joints. While higher Bi % is higher risk for EM, in the case of the functional notebook, it does not appear to have increased Bi migration tendency.

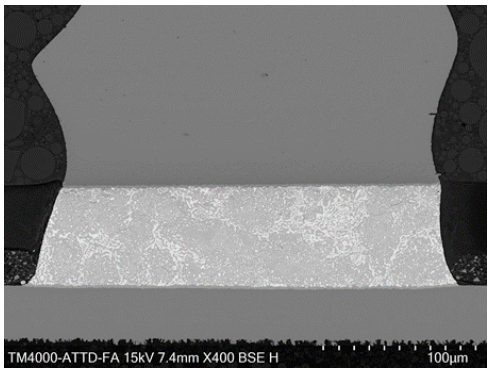

Figure 10. System B power FET switch pin after 2.5 years of daily corporate use.

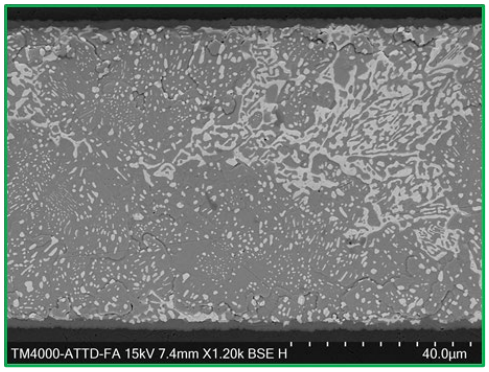

Figure 11. 1200X view of System B power FET solder joint microstructure. Note the presence of large amounts of Bi compared with the as built and System A

Table 4. Comparison of the as built and System B solder joint composition

	Approximate System Solder Joint Composition (wt%)	
Element	As Built	System B
Sn	58.35	59.56
Bi	20.06	40.44

CONCLUSIONS AND RECOMMENDATIONS

A significant amount of electromigration data reported in the literature has been based on eutectic SnBi solder. The use of eutectic SnBi allows results to be compared across both studies and solder paste suppliers. For actual electronic system designs, however, dopant modified paste metallurgies can provide enhanced margin against EM induced failures. When selecting an LTS solder paste, options employing Ag, Cu, Ni, and Sb can provide both EM benefits as well as improved thermal-mechanical performance. The functional systems evaluated in this work were assembled with LTS pastes using a selection of these dopants. While a paired comparison with SnBi is not possible, doped paste can be seen to have low risk of EM in an extended use case scenario. Products with lower Bi % are lower risk for EM, but offer less margin if hot tear elimination is required due to the higher peak reflow temperatures.

EM failure modes demonstrated in test vehicles such as lap shear joints, land grid array (LGA) sandwich solder joints, etc. can be recreated in functional notebook systems using similar accelerated current densities and temperatures. In the case of thin bottom terminated solder joints under accelerated conditions, localized melting and associated IMC growth, rather than EM driven Bi accumulation appears to be the dominant risk mode.

For production systems, knowledge of expected steady state current densities, motherboard temperatures, and likely use cases are key inputs for EM risk assessment. While design requirements will vary greatly, examination of post-service systems has shown that solder joint microstructure evolution may evolve rather slowly and EM related failure modes may not be a significant consideration.

Given the need for accurate data on expected current densities and solder joint temperatures in use case scenarios, it would be valuable to develop methods to quantify actual solder joint temperatures during operational cases rather than the chassis or global motherboard temperatures. As well, for high-risk components such as power FETS in higher temperature/current density applications, it will likely be necessary for component suppliers to develop solutions that allow current densities and solder joint temperatures to be more effectively managed.

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