Design for Manufacturability – Perspectives from a Manufacturing Engineer

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ABSTRACT
The quality and reliability of printed circuit board assemblies (PCBAs) is highly dependent upon the PCB fabricator and the PCB assembler. However, PCB design also plays a critical role and can have a significant impact on the success or failure of the manufacturing suppliers.

Today, designing and manufacturing PCBAs is increasingly difficult due to higher lead-free processing temperatures, the increasing density of electronic assemblies, and the use of smaller and smaller components. Not only does this create challenges for PCB designers, but it also increases the complexity of the PCBA manufacturing processes and puts additional demand on those manufacturing suppliers.

This paper will examine a few key areas of PCB design and manufacturing that can have a substantial impact on product reliability and how to mitigate reliability risks by deploying design for manufacturability (DFM) best practices. It will also explore the dependencies between the design and manufacturing processes.

Key words: DFM, PCB Design, PCBA Design

INTRODUCTION

DFM for printed circuit boards and printed circuit board assemblies ensures that electronic products can be consistently built with the minimum number of defects. Decreasing the number of defects not only reduces costs associated with building the product, but it will also result in positive reliability impacts. A good DFM process helps to identify manufacturing related issues with the product early in the design stage, where it is estimated that over 70% of the manufacturing costs are determined [1].

DFM is often overlooked in the design process. This can be because the PCB designer has little insight into the manufacturing processes used to build the product, whether that be internal or external. It may also be due to a lack of feedback from manufacturing partners or because the feedback only consists of simple design rule checks that are not necessarily tied back to the manufacturing process.

Successful DFM efforts require the integration of product design and process planning. The best DFM process has good insight into how the product runs in an actual manufacturing environment. A culture that is supported and sponsored by management is also required to implement a successful DFM process. Products need to be designed to the limitations of the manufacturing process. If new processes or techniques are required, the risks associated with them should be fully assessed. DFM should be considered for both bare PCBs and PCB assemblies, and should also incorporate requirements for test, rework and serviceability. DFM reviews should be conducted in conjunction with manufacturing sources. Implementation of a successful DFM process will result in reduced product costs by improving manufacturability upfront as illustrated in Figure 1.

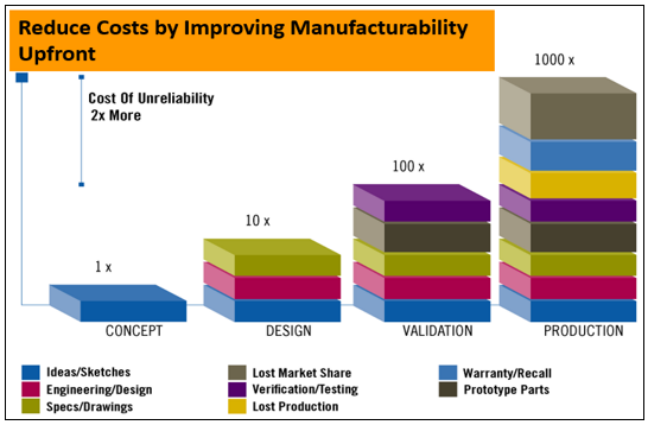

Figure 1. DFM Cost Benefits

SELECT DESIGN FOR MANUFACTURABILITY TOPICS

The remainer of this paper will explore several common DFM topics that will inevitably be encountered in designing today's electronic assemblies. It will examine the design and trade-offs decisions that must be considered to enhance the manufacturability of the assembly.

QFN Manufacturability

QFN (**Q**uad **F**lat Pack **N**o Lead or **Q**uad **F**lat **N**on-Leaded) packages like those sown in Figure 2 can pose many manufacturing and reliability challenges, but they have become very popular on today's electronic assemblies. There are many reasons for their popularity. For one, they are smaller, lighter, and thinner than comparable leaded packages, providing greater functionality per volume. The component manufacturer can get more IC's per frame, and they take up less PCB real estate, both of which reduce costs. The parts have no leads, so the traditional issues with lead coplanarity are avoided and due to their smaller size, they are generally available in tape and reel, making presentation to pick and place equipment more desirable. QFNs also offer better thermal performance than their leaded counterparts.

They have a more direct thermal path with larger area and their junction-to-ambient thermal resistance (θJa) is about half of a leaded counterpart. This allows for a 2X increase in thermal dissipation. Finally, the inductance of a QFN is about half of its leaded counterpart because it eliminates gullwing leads and shortens wire lengths, making them popular in RF designs.

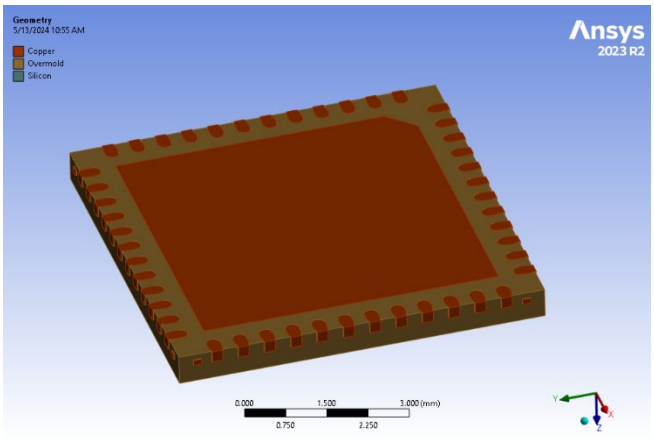

Figure 2. QFN Component

One downside of QFN components is that their solder fatigue life is reduced as compared to their leaded counterparts, mainly due the fact that they have reduced compliance (with no leads). This is important when considering them for use on products that will see significant thermal cycling in the field (See Figure 3).

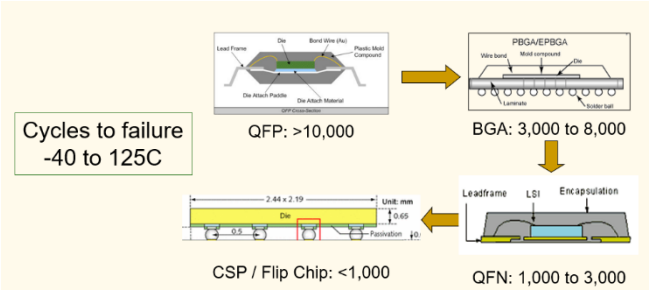

Figure 3. Package Cycles to Failure

One of the primary manufacturing challenges on these packages is how to handle soldering of the thermal pad. If too much solder paste is printed onto the thermal pad, the package can float or tilt, resulting in opens and/or bridges on the signal pins or excess solder can be expelled from the thermal pad during reflow leading to bridging on the signal pins. Not enough paste can lead to excessive voiding on the thermal pad. A good rule of thumb is to paste approximately 50%-70% of the thermal pad area with paste.

Voiding is always seen on the thermal pads of QFN devices and tends to be one of the biggest concerns for the manufacturing engineer. The thermal pad helps to dissipate heat from the chip into the PCB. If this is critical to the function of the design, the assembler should be made aware of this. It is prudent that thermal calculations be carried out to determine the minimum coverage area to allow for proper heat sinking. There are no industry standards for acceptable voiding on the thermal pad and a lack of published data that correlates the impact of voiding on the thermal pad to thermal performance [2]. IPC-A-610H considers voiding on the thermal pad that is more than 50% as a process indicator for Class 2 and 3 products in lieu of any other established voiding criteria between the user and the manufacturer.

There are many factors that affect the amount of voiding on QFN thermal pads including the footprint design, manufacturing process parameters, and the parts themselves. Voiding varies greatly depending on package type and even within a package type. Many common process variables such as reflow temperature or reflow atmosphere seem to have little effect on voiding levels [2].

One PCB design parameter that can have significant on thermal pad voiding is the construction of the vias on the thermal pad. The thermal vias can be open on both sides of the board, plugged with soldermask, or tented with soldermask. Plugging or tenting the vias from the opposite side of the board can exacerbate voiding on the thermal pad of the device, and tenting or plugging the via from the device side can leave bumps which can lead to difficulties in solder paste printing. In general, open vias result in less voiding because they provide a path for outgassing, but some of the solder can (and will) wet down the open via. While this leads to less voiding, it can create additional problems.

When the solder wets down the via, it tends to pull the package down closer to the PCB pad, resulting in diminished solder bond thickness between the signal pins and their pads. The extent of this pull-down (and therefore the resulting solder bond thickness) is dependent on both the size and the quantity of the vias. For products that will see significant thermal cycling, this reduced solder thickness will reduce reliability due to solder joint fatigue. Figure 4 shows the impact of solder bond thickness on characteristic QFN solder joint life for several different QFN packages (thermal cycle of -40ºC to 93ºC).

Another potential issue with open vias is that when the solder wets down the hole, it can lead to solder bumps on the opposite side of the board. These bumps can be large enough that they will act to hold the solder paste stencil away from the board surface during second pass printing which can lead to excessive paste deposition and solder bridging. It can also result in a damaged stencil. One design solution to this concern is to limit the placement of QFNs (or any other devices with open vias in soldered pads) to the second pass reflow side of the assembly. Another solution is to isolate the via from the rest of the thermal pad with a soldermask ring around the via (See Figure 5). While this does not completely eliminate solder in vias because the solder can migrate across the device thermal pad, it has proven to be successful in eliminating bumping on the opposite side of the board. It

does however reduce the solderable real estate on the thermal pad of the board, so this needs to be considered.

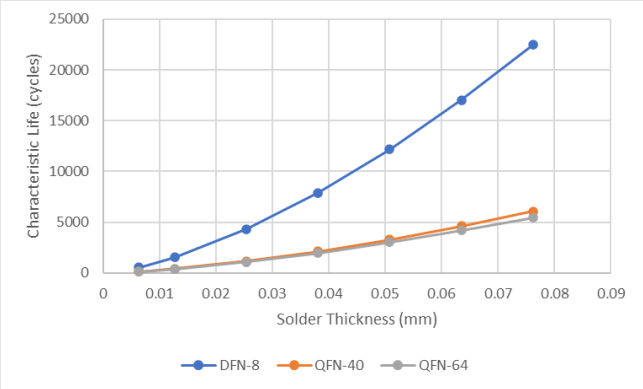

Figure 4. Characteristic QFN Solder Joint Life

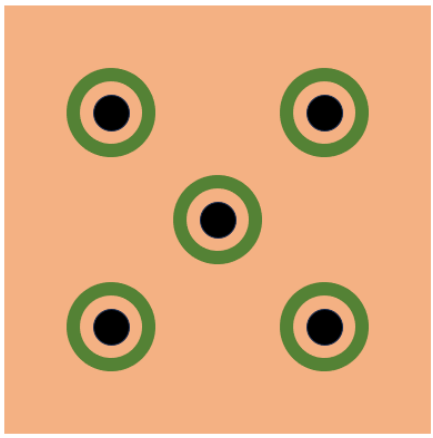

Figure 5. Soldermask Rings on QFN Thermal Pad

There is one additional issue that can arise with open vias on a QFN thermal pad. Some QFN devices have soldermask that defines the thermal pad on the device (See Figure 6). This can result in total starvation of solder on the thermal pad because the solder has the tendency to wet the board and the via before the solder wets the thermal pad on the device. While this doesn't occur 100% of the time, it can be a significant problem. Also, without some sort of x-ray inspection, one may not even be aware of this condition.

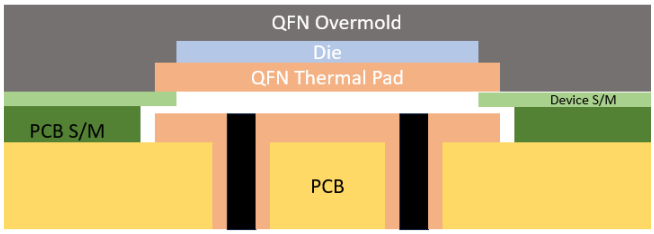

Figure 6. QFN w/Soldermask Defined Thermal Pad

While tenting the via(s) with soldermask would seem to be a good solution to this problem, one needs to be aware that the larger the via, the more difficult it is going to be to get a tent to successfully plug the via and prevent solder from escaping down the hole.

One foolproof way to eliminate these issues is to use vias that are filled and plated over with copper (so called VIPPO vias). Because there are no open holes, all of the issues discussed above with open vias are eliminated, as are those associated with soldermask plugged or tented vias. While this is a more robust solution, it does increase the cost of the PCB, which can be an issue for cost sensitive products. This process also adds thickness to the copper which can be a problem with very fine lines and spaces.

Now, let's discuss some other general QFN footprint recommendations. Pad widths for the signal pins on the board should be as wide as possible while still maintaining the ability to hold a soldermask web between the pads. There is an increased risk for bridging on the signal pins without soldermask between the pads. This becomes especially true as the pad pitch becomes smaller (specifically, 0.5 mm pitch and below). For a 0.5 mm pitch part, a 0.3 mm wide pad with a 0.05 annular soldermask opening around the pad can be used to ensure a 0.1 mm soldermask web between the pads. This should be within the capability of most quality PCB suppliers. Similarly, a 0.4 mm pitch part can use a 0.2 mm wide pad, a 0.05 mm soldermask opening around the pad, and the same 0.1 mm soldermask web between the pads.

Pad lengths are usually designed such that the inside edge of the PCB pad coincides with the inside edge of the package pad, but the pad extends out beyond the edge of the package. In practice, the PCB pad lengths recommended in the component datasheets are usually acceptable. Pad size for the center thermal pad should follow the part supplier's recommendation. Generally, a non-soldermask defined pad is preferred.

One strategy that has been deployed to improve the printability of the pad is to overprint the length of the pad to the outside of the package. This improves the stencil aperture ratio (with the longer printed pad) and it provides for more solder volume to the joint. The one thing to be cognizant of here is that other wettable surface features (such as open vias) should be sufficiently set back from the edge of the PCB pad.

PCB Assembly Panelization

Panelization of PCBs is a means of connecting multiple, individual PCBs together so that they can be processed by today's modern SMT equipment. Panelization at the PCB design stage is often overlooked and can be left in the hands of the PCB fabricator who has no insight into the type of equipment the panel will be processed on nor the type and location of components that will be used on the PCBA. The PCB fabricator's main goal in PCB panelization is to maximize the number of individual panels that can be achieved on a single fabrication panel. While this is certainly an important factor as it reduces the overall board cost, it is not the only thing to be considered. Improper panelization of the PCB can lead to assembly difficulties, yield problems, and potential reliability issues.

Most modern SMT equipment requires that the PCB panels have continuous, opposite handling edges with adequate clearances to SMT parts. The PCB/panel must also be of a minimum width to be properly handled on the equipment. PCBs that are odd shaped, too small, or lacking sufficient clearances to components on the handling edges of the board will need to be panelized in some manner to be run down the SMT line. In some high-volume manufacturing cases, panelization is used to increase the efficiency/output of the SMT line.

Fixturing the PCB through the SMT line is an option, but this approach does have some drawbacks. Fixtures can be quite expensive and many of them may be required so that the efficiency of the SMT line is not impeded. The fixture will need to be maintained to function properly, and fixturing PCBs also tends to complicate the SMT stencil printing operation. Fixturing of multiple boards that are not panelized will almost certainly lead to alignment issues at the solder paste print operation, as it is very difficult to get the required alignment between multiple, unconnected PCBs and a single stencil. In some cases, fixturing is inevitable such as when the PCB is very thick or very thin and cannot be handled due to limitations of the SMT equipment. Small boards will need to be panelized even if they are ultimately processed in a fixture.

The preferred panel option is no panel at all. In this case, the PCB is sufficiently large, it has opposite, continuous handling edges, clearances to all SMT components on the handling edges is sufficient, and the PCB is adequately thick (but not too thick). If these requirements are met, the PCB can be processed as is, fixtures can be avoided, and no downstream depaneling equipment is needed.

In the event PCB panelization is needed, there are three primary methods typically used. They are 1) v-score, 2) perforated tab and route, and 3) solid tab and route. Each of these methods will be discussed here.

V-Score

For v-score panelization, a V-shaped groove is cut into the top and bottom board surface between the individual boards. The score depth is typically about 1/3 of the board's thickness, so roughly 1/3 of the board's thickness remains to hold the panel together (See Figure 7).

A piece of equipment commonly referred to as a pizza cutter (Figure 8) is typically used to singulate the panel into the individual boards. The panel can also be taken apart manually by breaking the board at the v-score.

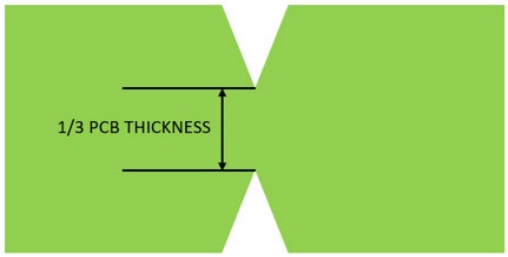

Figure 7. V-Score Panel

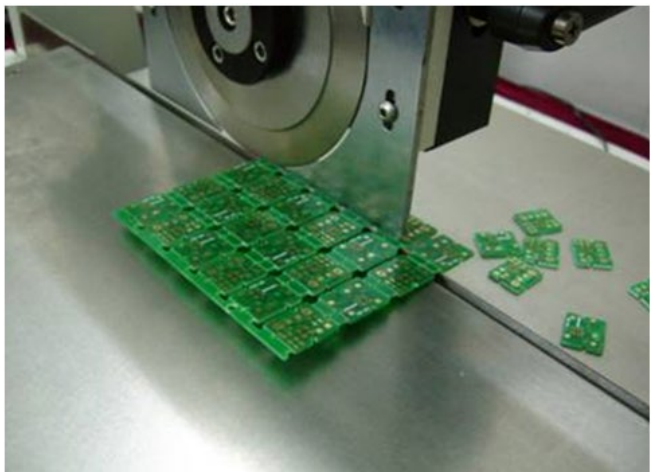

Figure 8. V-Score Depanelization

The primary concern with v-score panelization is that fragile components such as multilayer ceramic chip capacitors (MLCCs) that are too close to the v-score can very easily be damaged during the singulation process, whether that be done with a pizza cutter or manually. These fragile parts can easily be cracked due to the stress applied during singulation. This can result in immediate failure of the device, or it can go undetected and eventually lead to field failures as the parts/cracks are exposed to the field environment. There are other limitations to v-score panels. The V-score must be in a straight line, it does not leave a smooth board edge, and parts that overhang the board edge such as connectors cannot be used. The panels are also inherently weak so the panel can come apart prematurely making assembly difficult or impossible. For these reasons, v-score panelization should only be used on the simplest of PCB designs.

Some of these concerns with v-score panels can be alleviated by using jump scoring to make the panel less fragile or by using a combination of v-score and pre-routing near fragile components for cost-sensitive products where the cost associated with other depanelization methods are important. Figure 9 shows an example of both. The v-scores do not extend to the edge of the panel in the horizontal direction. This acts to impart some rigidity to the panel. The panel also has pre-routes along the edge in the vicinity of fragile devices to help from damaging the parts during the singulation process. The use of the pre-routes does however necessitate the use of more PCB material.

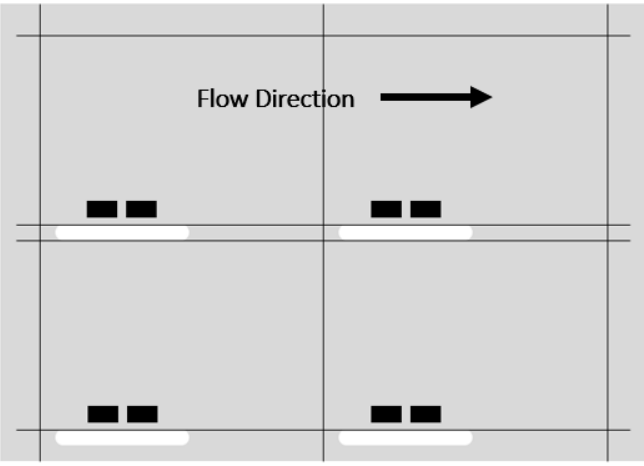

Figure 9. Jump Score and Combination V-Score and Pre-Route Panel

Perforated Tab and Route

Perforated tab and route panels use pre-routed channels and connected tabs between the boards and/or between the boards and the waste areas on the panel. The connected tabs have holes drilled into them so that the board material left can easily be broken apart. An example of a connected tab is shown in Figure 10. The boards can be separated from the rest of the panel manually or with an automated router. Manual separation is usually carried out with the use of a fixture, but in some cases, they are broken apart by hand.

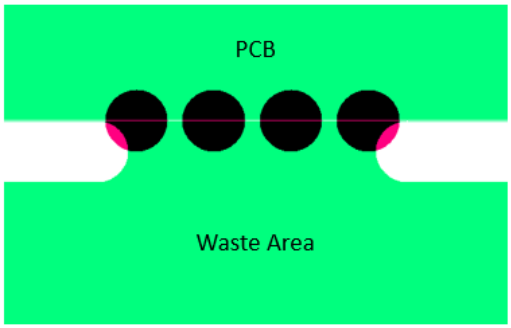

Figure 10. Perforated Tab and Route Panel

Manual separation of perforated route and tab panels suffers from some of the same concerns as v-score panels. Fragile parts that are too close to the connecting tabs can easily be damaged during singulation. The panel needs to be properly designed if manual separation is going to be used. The connecting tabs that are to be broken must all be in the same axis, otherwise board damage can occur. Care must be taken on properly locating the connecting tabs so that overhanging parts and fragile parts are avoided. Figure 11 shows a configuration that would be acceptable for a perforated tab and route panel so that it could be manually separated. It is possible to use an automated router to separate the boards, but this makes the use of the drilled holes in the connected tab unnecessary. In fact, the holes only act to make the panel weaker, and much like the v-score panel, can lead to unwanted separation of the boards prior to completing assembly. Also, the board edge that remains can be jagged at the connecting tabs, so this method is not advisable where a smooth board edge is desired.

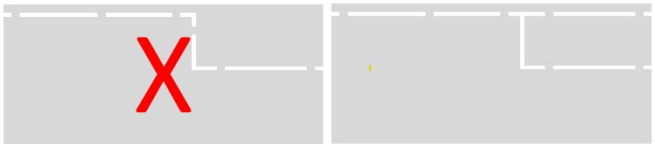

Figure 11. Perforated Tab and Route Panel Configuration

Solid Tab and Route

Solid tab and route panels are very similar to perforated tab and route panels, with the exception that there are no drilled holes in the connected tab (See Figure 12). These panels are intended to be separated with an automated router and cannot be manually separated. Routing is generally done with a traditional router bit system, but laser routing can also be used with sufficiently thin boards. The panels are normally loaded into a router fixture for the singulation process, but in-line routing without fixturing is common for high volume applications. Whether it be in-line routing or routing using a fixture, the panel must be properly configured with tooling holes and other features so that the panels and the individual boards can be properly held in place during the routing operation.

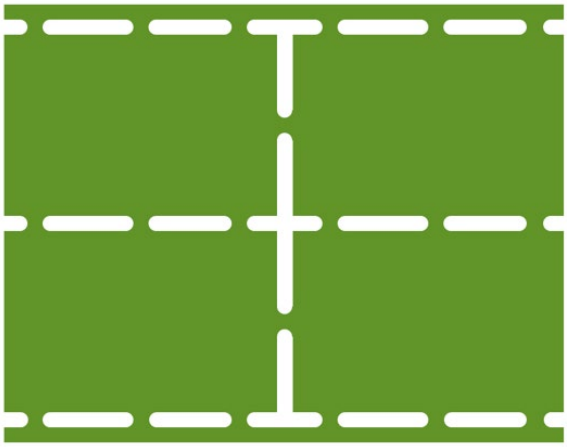

Figure 12. Solid Tab and Route Panel

Because there is no manual singulation, the process is much better controlled and repeatable, and parts and traces can be much closer to the edge of the board than with other panel methodologies. With careful attention to the panel design, overhanging parts can also be accommodated. If boards require panelization for any reason, the solid tab and route panel is the safest and most preferred method. Because of the type of equipment and fixturing involved, it is also the costliest.

Damaging fragile parts such as MLCC during the singulation process is a primary concern when considering assembly panel options. Regardless of the panel type used, it is prudent to characterize the mechanical stresses involved in the process with strain gauge testing. Literature suggest that board-level strain should be maintained below 750 microstrain (500 microstrain for LF assemblies) to avoid

flexure damage to MLCCs. The use of Flexiterm (Syfer) or Soft Termination (AVX) caps can also improve the robustness of an assembly with respect to flexure cracks [1].

PCB Via Protection Strategy

Plated through-hole vias are used in PCBAs to provide interconnect between the various components and layers of a PCB. There are many ways that these vias can be treated with respect to how soldermask is applied to them. The soldermask application can have a significant impact on PCBA manufacturability as well as the reliability of the finished product.

The most preferred treatment is to have an open via where there is a 0.003" soldermask clearance around the via hole as is shown in Figure 13. This construction allows the via to be effectively cleaned during PCB processing, especially with respect to after the surface finish is applied to the board. Most often, soldermask is applied to the PCB before application of the surface finish. Application of the surface finish involves cleaning of the base metal surfaces before the final finish so that solderability is maintained. When LPI soldermask is applied over the via (a process known as tenting) it results in a blind hole if only one side is covered, and a sealed hole if both sides are tented.

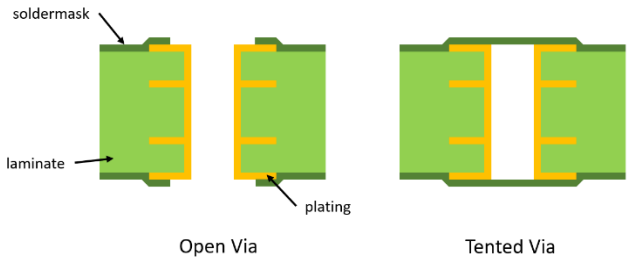

Figure 13. PCB Via Soldermask Treatment

The problem with this treatment is that holes or cracks in the soldermask "tents" covering the via can result. If these holes or cracks are present during cleaning of the PCB base metal and subsequent application of the surface finish, fabrication chemicals can be ingested into the via and cannot be properly cleaned out. This can result in corrosion in the plated through via which can then lead to thin plating and cracks in the via wall. This will ultimately result in opens during assembly processing (reflow) or thermal cycling of the final product. Figure 14 shows an example of this condition. This may be discovered at assembly test, but this condition also has the potential of making it into the field where the product can fail during thermal cycling that the product may encounter. The larger the via, the less likely that it will be tented without defects.

One additional problem that can be encountered with vias that are only covered with soldermask from one side of the board is test point contact issues at in-circuit test (ICT). If the via pad is to be used as an ICT test pad, it obviously needs to be free of soldermask. If soldermask is applied over the via on the opposite side of the board from the test point, soldermask can droop into the via hole and contaminate the test pad or prevent the ICT probe from making good contact with the pad (See Figure 15). These concerns are alleviated with open vias.

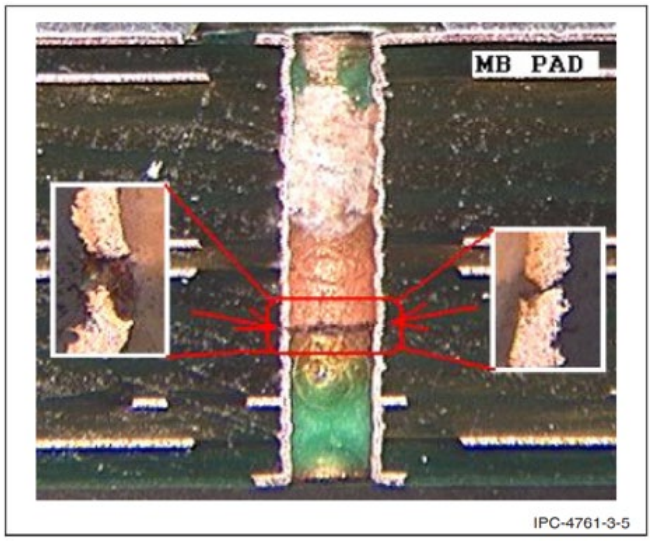

Figure 14. Corroded Hole Wall Plating (courtesy of IPC-4761)

However, the use of open vias in a PCB design does requires adherence to other design rules. If the via is connected to a trace that has an SMT component pad connected to it, the via must be sufficiently far away from the pad to assure an ample soldermask dam between the pad and the via is achieved. Otherwise, solder can flow down the via during SMT reflow, leaving the SMT pad with an insufficient or even open solder connection. A minimum soldermask dam of 0.004" – 0.005" is generally considered to be minimum that is required to avoid this condition. So, if the soldermask clearance to the via hole edge is 0.003" and the soldermask clearance to the SMT pad is 0.002", a 0.009" spacing is required between the via hole edge and the SMT pad to maintain the minimum soldermask dam of 0.004".

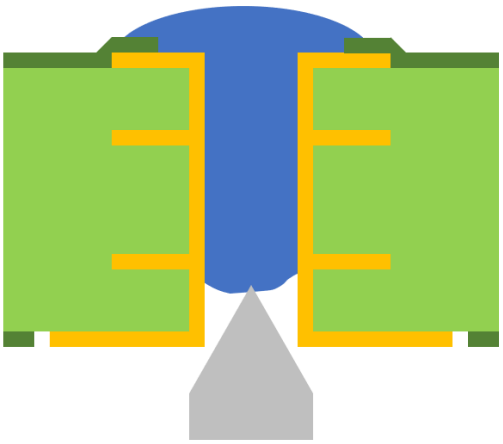

Figure 15. ICT Probe Contact Issue due to Soldermask Plug

There are other soldermask treatments that can be applied to the vias. If the PCB does require that the vias be covered for some reason, soldermask plugs can be added to the vias. If this strategy is used the soldermask plugs should be applied to the board after application of the surface finish to avoid the via contamination issue discussed earlier. This requirement should be explicitly stated on the PCB fabrication drawing. This may also limit the surface finish selection for the board as the soldermask plugs need to go through a curing process which could cause solderability issues with OSP or immersion tin finishes.

There are additional concerns with soldermask plugged vias. If the bump heights become excessive, they can hold up the solder paste stencil and prevent getting a good seal around the SMT pad which can lead to excessive paste deposition and potential solder bridging. This is especially problematic in areas of high via concentration such as BGA devices. Maximum plug height above the board surface should be documented in the fabrication drawing. The plug depth into the hole should also be well controlled if it is applied to a via on the opposite side of the board from an ICT point due to the same ICT test probe concerns discussed earlier.

CONCLUSION

The deployment of a DFM process by electronics product designers is an excellent way to improve both the manufacturability and reliability of their products. Careful consideration of DFM best practices should have a positive impact on overall product cost and reliability which will ultimately lead to improved customer satisfaction.

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