A Comparison of Thermal Cycling and Thermal Shock for Evaluating Solder Joint Reliability

Richard Coyle[1], Dave Hillman[2], Chloe Feng[1], Tim Pearson[3], Michael Osterman[4], Jayse McLean[5], Joe Smetana[6], Keith Howell[7], Julie Silk[8], Hongwen Zhang[9], Jie Geng[9], Derek Daily[10], Anna Lifton[11], Morgana Ribas[12], Raiyo Aspandiar[13], Ranjit Pandher[5], Richard Popowich[1], James Wertin[14], Jean-Christophe Riou[15], Issac Becker[1,20], Grace O'Malley[16], Madan Jagernauth[17], Denny Fritz[18], Shantanu Joshi[19], and Jasbir Bath[19]

[1]Nokia Bell Laboratories, NJ, USA, [2]Hillman Electronic Assembly Solutions, IA, USA, [3]Collins Aerospace, IA, USA, [4]CALCE, MD, USA, [5]John Deere, ND, USA, [6]Nokia, TX, USA, [7]Nihon Superior Co., Ltd., Osaka, JP, [8]Keysight Technologies, CA, USA, [9]Indium Corp., NY, USA, [10]Senju Comtek Corp., CA, USA, [11]MacDermid Alpha Electronics Solutions, NJ, USA, [12]MacDermid Alpha Electronics Solutions, Bangalore, IND, [13]Intel, OR, USA, [14]Heraeus Electronics, PA, USA, [15]Safran Electronics and Defense, Valence, FR, [16]iNEMI, NC, USA, [17]HDP User Group, International, TX, USA, [18]Fritz Consulting, OH, USA, [19]Koki Solder America, OH, USA, [20]Rochester Institute of Technology, NY, USA

richard.coyle@nokia-bell-labs.com; crgdragon@gmail.com

ABSTRACT

The industry standard for accelerated temperature cycling, IPC-9701B, defines test conditions for characterizing solder interconnect fatigue. The document specifies a maximum cycling ramp rate of 20 °C/minute to avoid thermal shock conditions that can accelerate failure modes other than low cycle fatigue in the bulk solder. This investigation compares the performance and failure mode of two ball grid array (BGA) packages tested with cyclic ramp rates characteristic of thermal cycling and thermal shock. The accelerated temperature profile is from -40 °C to 125 °C for thermal cycling and thermal shock, with the cycling ramp rates approximately three times faster with thermal shock and with equal dwell times in cycling and shock. The test matrix includes BGA packages fabricated with eutectic SnPb and near-eutectic SAC305 solder alloys as the performance baselines, and three high-performance solder alloys based on the SAC system but modified with additions of bismuth (Bi) and antimony (Sb). The failure data are reported as characteristic lifetime η (the number of cycles to achieve 63.2% failure), slope β, and cumulative 1% failure from a two-parameter Weibull analysis. Destructive cross-sectional analysis was used to characterize the solder microstructures before and after testing and the interconnect failure mode. The results show that the thermal cycling ramp rate and the thermal shock ramp rate produced the same results quantitatively and the same failure modes. These findings apply to the two BGA components in combination with the five solder alloys used in the study. For these test conditions, components, and solder alloys, the same results were achieved in thermal shock compared to thermal cycling with a 30% savings in test duration.

Key words: Thermal cycling, thermal shock, Pb-free solder, high-performance solder alloys, thermal fatigue, failure mode, ramp rate, dwell time, solder microstructure

INTRODUCTION

Accelerated temperature cycling (ATC) tests are used to assess the influence of thermal changes on the reliability of electronic devices and assemblies. These accelerated tests are categorized as thermal cycling (TC) or thermal shock (TS) depending on the rate of temperature change or ramp rate in the test profile. Thermal cycling is the method used to evaluate the thermal fatigue performance of solder attachments in electronic assemblies. IPC-9701B [1], the industry specification for thermal fatigue life characterization of solder attachments, specifies a maximum ramp rate of 20 °C/minute for thermal cycling. This limit was established to avoid thermal shock that can induce excessive and stress-altering thermal gradients through the parts under test and accelerate failure modes other than the desired low cycle fatigue failure mode in the bulk solder. The 20 °C/minute maximum ramp rate was codified in the initial version of IPC-9701 in 2002, when eutectic SnPb was the preferred alloy for electronic manufacturing, and years before the widespread implementation of Pb-free solder assembly. Although JEDEC JESD22-104B [2] is cited less frequently

for interconnect testing, it specifies a preferred maximum rate of 10 °C to 14 °C/minute, which is consistent with IPC-9701B.

There is an incentive for using a temperature cycle test with a faster ramp rate because it could provide a significant saving in time and cost. Earlier completion of testing could enable a faster development cycle for products, but a thermal shock test must generate the expected thermally activated fatigue failure mode in the solder joints.

There is disagreement in the literature about the definition of thermal shock conditions and test parameters. It is challenging to interpret and compare data from the literature due to the wide range of major test variables such as temperature extremes, ramp rates, dwell times, component types, and solder alloy composition. More of the published work has been performed on SnPb solder rather than Pb-free alloys. Furthermore, there are other pertinent variables that limit comparisons such as solder assembly parameters, printed circuit board thickness and design features, and solderable final finish. Generally, increasing the ramp rate decreases the number of cycles to failure, but the following review of the published literature demonstrates the inconsistencies and disagreements in the data and its interpretation relative to the significance of the ramp rate effect.

Sastry et al. tested eight different SnPb ball grid array (BGA) packages using 0/100 ºC and -40/125 ºC profiles [3]. The 0/100 ºC profile had 10 ºC/min and 20 ºC/min ramp rates with 5 minute dwell times and the -40/125 ºC profile had a 16.5 ºC/min ramp rate with 5 minute dwell times. The dwell times were consistent for ramp rates from 10 ºC/min to 20 ºC/min, and with significant differences in temperature extremes and ΔT, but failure analysis showed the location of crack propagation was in the bulk solder and the failure modes were thermal fatigue in all legs of the experiment. It also is noteworthy that the 0/100 ºC profile, with the 20 minute cycle (20 ºC/min ramp rate) produced the same results based on characteristic lifetime as the 30 minute cycle (10 ºC/min ramp rate). Thus the 0/100 ºC profile, with the faster ramp rate coupled with the shorter dwell time of 5 minutes, produced the exact same results in eight different BGA packages with a 30% savings in test duration.

Ghaffarian and Kim [4] tested a fine pitch SnPb BGA using a -55/125 ºC profile with ramp rates of 2-5 ºC/min and 10-15 ºC/min and dwell times of 20 and 25 minutes, respectively. Although the faster ramp rate is below the ostensible 20 °C/minute thermal shock guideline, it produced failures three times faster than the slower ramp rate. The authors did not discuss if the long dwell times had affected the results, and there was no failure analysis to confirm that the failure mode was the same with both profiles.

Sahasrabudhe et al. [5] tested a large-body SnPb flip chip BGA (FCBGA) using a -55/125 ºC profile in thermal shock (72 ºC/min ramp rate with 15 and 30-minute dwell times) and thermal cycling (12ºC/min with 15 and 30 minute dwell times). They found that the thermal shock (faster ramp rate) and the longer dwell time reduced the number of cycles to failure. Failure mode analysis was not included in this paper.

deVries et al. [6] tested a SnPb 256BGA using a -40/125 ºC profile to compare thermal shock (40 ºC/min ramp rate with 8 to 10-minute dwell times) to thermal cycling (16 ºC/min ramp rate with 7 to 8 minute dwell times). They found that thermal shock decreased characteristic lifetime by 30%. They warned that "thermal shock could introduce different types of failures," but did not perform failure analysis on tested samples. Zhai et al. used a smaller SnPb 64BGA to compare thermal shock to thermal cycling [7]. The also used a -40/125 ºC profile and ramp rates close to those used by deVries, with a 33 ºC/min ramp rate for thermal shock and a 16.5 ºC/min ramp rate for thermal cycling, but with slightly shorter 5 minute dwell times. In contrast to the findings of deVries, Zhai reported no difference in cycles to failure between thermal shock and thermal cycling. The experimental results were correlated with finite element analysis, but no physical failure analysis was performed.

Qi et al. [8] used a 2512 resistor assembled with SnPb and SAC387 (Sn3.8Ag0.7Cu) solder alloys and a 0/100 ºC profile to compare thermal shock (95 ºC /min ramp rate) to thermal cycling (14 min/ ºC ramp rate), both with 5 minute dwell times. They reported minimal differences due to ramp rate in cycles to first failure (N1) or cycles to N63 for SnPb and SAC387. They also compared thermal shock with 0/100 ºC to thermal shock with -40/125 ºC. SAC387 had a higher N63 with 0/100 ºC, but SnPb had a higher N63 with -40/125 ºC. No failure analysis was performed for any of the tests.

Dusek et al. preconditioned Pb-free surface mount resistor solder joints using six different accelerated testing regimes (thermal cycling and shock) and shear tested them to failure [9]. They measured the most damage to the solder joints with a thermal cycling profile of -55/125 ºC with a 10 ºC/min ramp rate and 5 minute dwell times. Less damage was measured with a thermal shock profile of -55/125 ºC with a 55 ºC/min ramp rate and zero minute dwell times. The authors reported a subtle difference in failure mode with crack propagation clearly in the bulk solder with thermal cycling and in the solder but consistently extremely close to the intermetallic layer and component termination with thermal shock.

Hokka et al. [10] conducted a comprehensive evaluation of the effects of ramp rate and dwell time on thermal cycling performance of a 144BGA with SAC305 Pb-free solder attachments. Their profile was -40/125 ºC, and they used ramp rates of 24 °C/min for thermal shock and 8 °C/min for thermal cycling. Thermal shock and thermal cycling also included dwell time variables of 0 and 30 minutes. Their results show that the increase in ramp rate (TS) decreases the N63 cycles to failure by 31% for the zero minute dwell time, and the increase in ramp rate (TS) decreases the N63 cycles to failure by 21% for the 30-minute dwell time. The authors comment that their experimental evidence on the effects of

ramp rate on the cycles to failure agrees with much of the literature, namely increased ramp rate decreases the cycles to failure significantly.

As a companion to their work on the effect of test parameters, Hokka et al. [11] published a paper focused on the relationship between failure mode and harsh loading conditions. In accelerated tests, they report that the microstructure evolves by recrystallization of the Sn with crack propagation along intergranular paths. However, under milder, nonaccelerated, service conditions, the microstructure evolves slowly without recrystallization, which results in transgranular crack propagation through the solder. These findings suggest that the typical thermal cycling tests used to solder interconnect reliability do not accelerate the same failure mechanism that occurs in real-use service conditions. This is consistent with Grossman and Weber [12] who state that different deformation rates can cause different deformation mechanisms to occur. They assert further that thermal shock tests that shorten the test time can activate deformation mechanisms that do not occur in practice.

In summary, the literature review indicates that faster ramp rates tend to decrease the cycles to failure significantly. Faster ramp rates are associated with thermal shock testing, although for interconnect testing, thermal shock conditions are not as well-defined as those for thermal cycling. Quantitative comparisons are challenging because the data in the literature originate from a variety of cycling tests that are conducted using vastly different ramp rates, cyclic temperature ranges (ΔT), temperature extremes, and dwell times. Dwell time is a factor in thermal cycling and has been studied systematically for SAC alloys [13], but the literature is not clear with respect to dwell effects in thermal shock or for high-performance alloys. A lack of failure mode analysis also limits the value of certain test results from the literature, and it would be beneficial to have more data comparing thermal shock to thermal cycling for Pb-free interconnects.

In this investigation, the performance and failure mode of two ball grid array (BGA) packages are compared using ramp rates typical of thermal shock and thermal cycling. The basic cycling profile is from -40 °C to 125 °C with the cycling ramp rates approximately three times faster with shock and with equal dwell times in cycling and shock. The BGA test matrix has packages fabricated with SnPb and SAC305 solders as performance baselines, which are compared to three high-performance solder alloys based on the SAC system but modified with additions of bismuth (Bi) and antimony (Sb). The alloy compositions are shown in (Table 1). Post-cycling cross-sectional analysis was used to characterize failure modes.

Table 1. The nominal compositions of the solder alloys used for the thermal cycling and thermal shock comparison.

Alloy	Nominal Composition (wt. %)						
	Sn	Ag	Cu	Bi	Sb	In	other
SAC305	96.5	3.0	0.5				
SnPb	63.0						Pb 37.0
M794	89.7	3.4	0.7	3.2	3.0		Ni
Indalloy 279	89.3	3.8	0.9		5.5	0.5	
LF-C2	92.5	3.5	1.0	3.0			

Experimental

Test Vehicle

Component and Test Board Descriptions

This study utilizes the components and printed circuit board (PCB) developed as the test vehicle for the iNEMI Alloy Alternatives project [13]. The two daisy-chained ball grid arrays (BGA), a 192 I/O chip array BGA (192CABGA) and an 84 I/O thin core chip array (84CTBGA) are shown in Figure 1 [14]. The SnPb and SAC305 ball grid arrays were purchased as off-the-shelf components. The high-performance alloy ball grid arrays were purchased as land-grid arrays (LGA) to enable subsequent attachment of each of the different high-performance Pb-free-alloy balls included in the scope of the program (Table 1). The ball attachment was performed at SemiPack (https://www.semipack.com) using the process developed for the iNEMI Alternative Alloys project [13, 15-19].

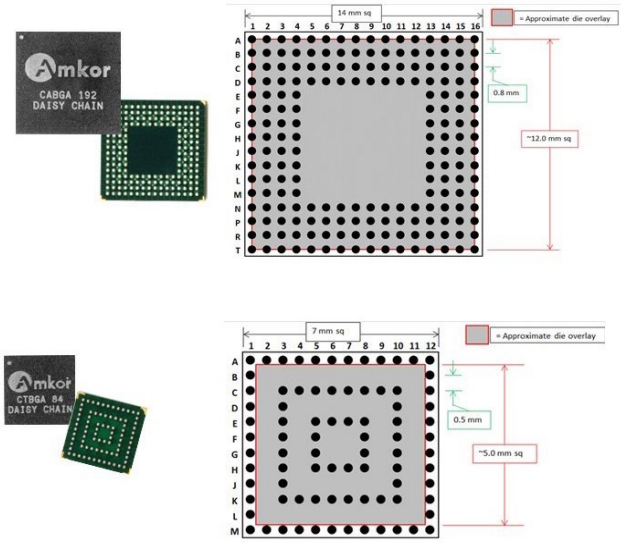


Figure 1. The pin diagrams with die overlay for the 192CABGA and 84CTBGA daisy chained components.

The printed circuit board (PCB) test vehicle is 2.36 mm (0.093 in.) thick, with a 6-layer construction with 16 sites for the larger 192CABGA, and another 16 sites for the 84CTBGA (Figure 2). The boards are fabricated with the Panasonic R-1755V high temperature laminate material and the final finish is a high temperature organic solderability preservative (OSP). The complete attributes of the components and PCB are provided in Table 2.

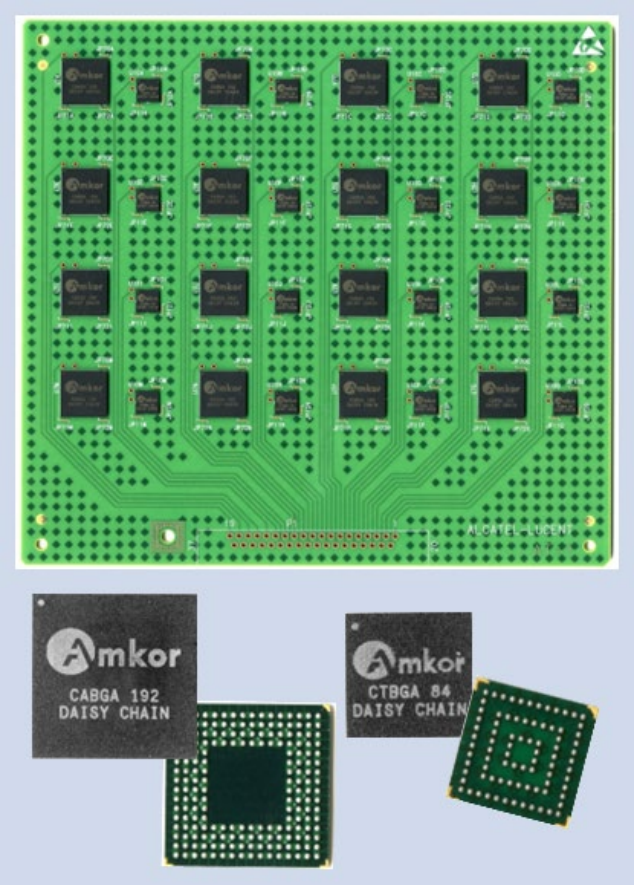


Figure 2. A fully populated, daisy chained test vehicle.

Table 2. BGA package and PCB attributes.

BGA Package Attributes		
Designation	192CABGA	84CTBGA
Die Size	12x12 mm	5x5 mm
Package Size	14x14 mm	7x7 mm
Ball Array	16x16	12x12
Ball Pitch	0.8 mm	0.5 mm
Ball Diameter	0.46 mm	0.3 mm
Pad Diameter	0.381 mm	0.3 mm
Pad Finish	Electrolytic Ni/Au	Electrolytic Ni/Au
Au thickness	0.6 µm	0.6 µm
PCB Attributes		
Dimensions	165 x 178 x 2.36 mm	
Laminate	Panasonic R-1755V	
Surface Finish	Entek HT OSP	
No. Cu Layers	6	
Pad Diameter	0.356 mm	0.254 mm
Solder Mask Dia.	0.483 mm	0.381 mm
Laminate	Panasonic R-1755V	
Glass Transition Temperature, T_g	165 °C	
Decomposition Temperature, T_d	350 °C	
Room Temperature Storage Modulus	11.6 Gpa	

Solder joint attachment reliability is dependent strongly on the coefficient of thermal expansion (CTE) mismatch (difference) between the package and the PCB as well as the distance from neutral point (DNP) [20]. Although the small chip array package sizes used in this study minimize the DNP effect, their large die to package ratios (DPR) result in substantial CTE mismatch [20]. The modulus or stiffness of the PCB also can affect solder joint reliability.

The CTE of the PCB was measured using a thermomechanical analyzer (TMA) and the composite coefficients of thermal expansion of the BGA packages were measured using microscopic moiré interferometry. The data in Table 3a show a lower composite CTE for the 192CABGA package. The lower CTE of the 192CABGA results in a larger CTE mismatch with the PCB, hence the thermal cycling lifetime of the 192CABGA is shorter than that of the 84CTBGA [14-18]. The CTE data for the PCB laminate material are shown in Table 3b.

Table 3a. CTE of the BGA component test vehicles measured by microscopic moiré interferometry.

BGA Package	Effective CTE α (ppm/°C) T °C:24~130	
	x-direction	y-direction
192CABGA	8.6	10.1
84CTBGA	10.9	11.0

Table 3b. The CTE of the printed circuit board fabricated with Panasonic R-1755R laminate material.

Printed Circuit Board Laminate	Effective CTE α (ppm/°C) T °C:20~140	
	x-direction	y-direction
Panasonic R-1755V	13.5	16.1

Test Vehicle Surface Mount Assembly

The solder assembly of the test vehicles was performed at Collins Aerospace, Cedar Rapids, IA. A pilot build using SAC305 components and paste was conducted to establish the stencil printing and reflow process parameters. A 5-mil (125 µm) thick stencil was used with 14 mil (0.35 mm) diameter round apertures for the larger 192CABGA and 12 mil x 12 mil (0.3 mm x 0.3 mm) square apertures for the smaller 84CTBGA. The test vehicles were reflowed in a 14-temperature zone convection oven in a nitrogen atmosphere. Type 4 no-clean solder paste was used for all the final assemblies. The nominal peak temperature measured on the board adjacent to the solder joints was 245 °C [21].

Accelerated Temperature Cycling

Thermal Cycling and Thermal Shock

The daisy-chained components and the test circuit boards enabled electrical continuity testing after surface mount assembly and in situ, continuous monitoring during thermal

cycling. The solder joint resistance was monitored using event detectors set at a resistance limit of 1000 ohm. The failure data was reported as characteristic life η (the number of cycles to achieve 63.2 % failure), slope β, and cumulative 1% failure from a two-parameter Weibull analysis. Each alloy test cell contains two fully populated replicate test boards to provide a sample size of 32 BGA components of each type for thermal cycling and an additional populated test board for baseline quality and microstructural characterization.

Thermal cycling was done in a single zone chamber, and thermal shock was done in a vertical, dual zone, air-to-air chamber. The profiles for **thermal cycling** and **thermal shock** are shown in Figure 3 and Table 4. Both profiles have 15-minute upper and lower temperature dwell times, resulting in cycle times of 60 minutes for thermal cycling and 40 minutes for thermal shock. This corresponds to cyclic frequencies of 24 and 36 cycles per day, respectively.

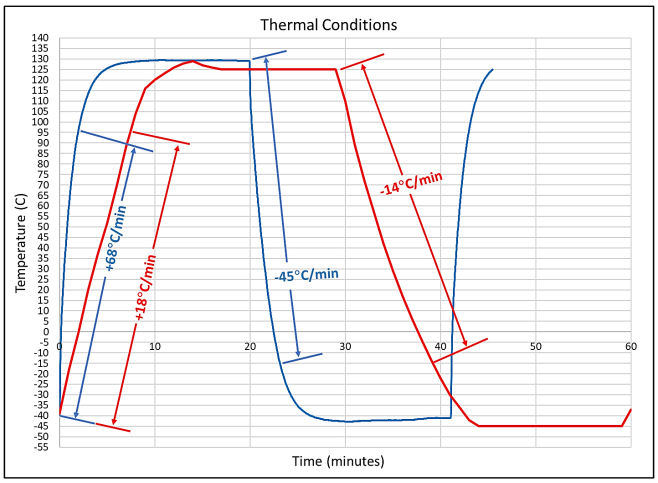


Figure 3. Accelerated temperature cycling profiles for **thermal cycling** and **thermal shock**.

Table 4. Accelerated temperature cycling ramp rates and cycle times for **thermal cycling** and **thermal shock.**

	Thermal Cycling	Thermal Shock
Ramp rate -40 to 125 °C	14 °C/minute	68 °C/minute
Ramp rate 125 °C to -40 °C	18 °C/minute	45 °C/minute
Dwell time 125 °C	15 minutes	15 minutes
Dwell time -40 °C	15 minutes	15 minutes
Total cycle time	60 minutes	40 minutes

Microstructural Characterization and Failure Analysis

Destructive cross-sectional analysis (metallography) and scanning electron microscopy (SEM) are used to document the solder joint quality and basic solder microstructures of representative board level assemblies from each of the component and alloy test cells. The baseline characterization before temperature cycling enables microstructural comparisons to samples selected for failure mode analysis after temperature cycling. The SEM operating in the backscattered electron (BSE) imaging mode is effective for differentiating phases in SAC microstructures [15-19, 22], but more sophisticated methods are required to detect and quantify certain phases in the high-performance alloys [23-25].

RESULTS

Solder Joint Characterization

Figure 4 shows low magnification BSE images of time zero (baseline) 192CABGA and 84CTBGA solder joints. The solder joints have acceptable assembly quality with no discontinuities or cracking at the soldered interfaces. There is a minor amount of shrinkage porosity on the surfaces of some solder spheres.

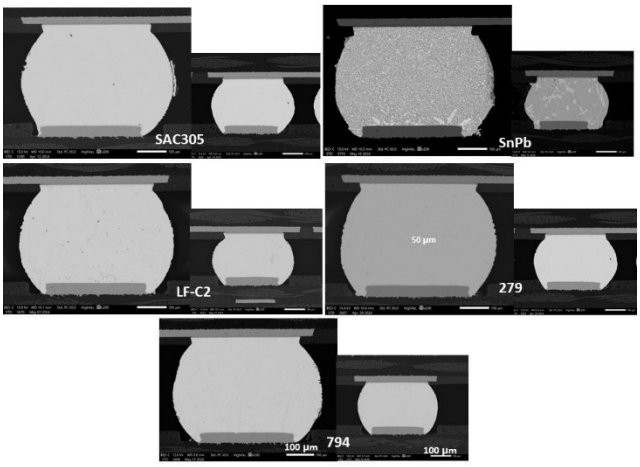


Figure 4. Low magnification BSE images of typical as-assembled solder joints for the five alloys in this investigation. The larger images are the 192CABGA and the smaller images are the 84CTBGA,

Accelerated Temperature Cycling

Thermal Cycling and Thermal Shock

The bar charts in Figure 5 and Figure 6 can be used to compare the characteristic lifetimes of the 192CABGA and 84CTBGA in thermal shock and thermal cycling. The complete Weibull statistics are provided in Table 5 and Table 6. Various supplemental Weibull plots are provided in Appendix A.

The data from the bar charts and tables show clearly that the three high-performance solder alloys outperform SnPb and SAC305 by significant margins in thermal shock and thermal cycling with both BGA components, in terms of characteristic lifetime and 1% cumulative failure. This result was anticipated based on previous cycling data with these alloys and the two BGA test vehicles [16-19, 21].

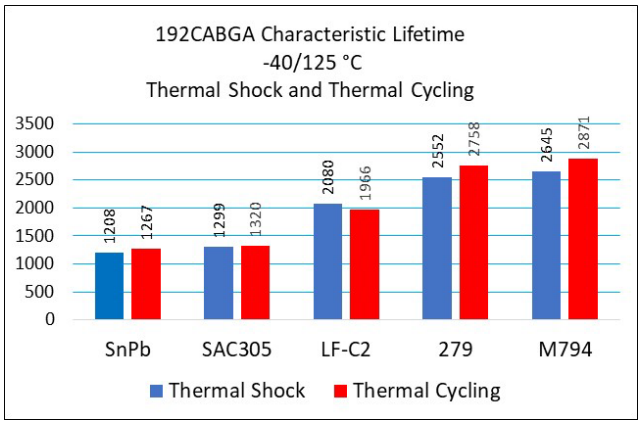


Figure 5. A bar chart comparing the characteristic lifetimes in **thermal shock** and **thermal cycling** for all alloys with the 192CABGA component.

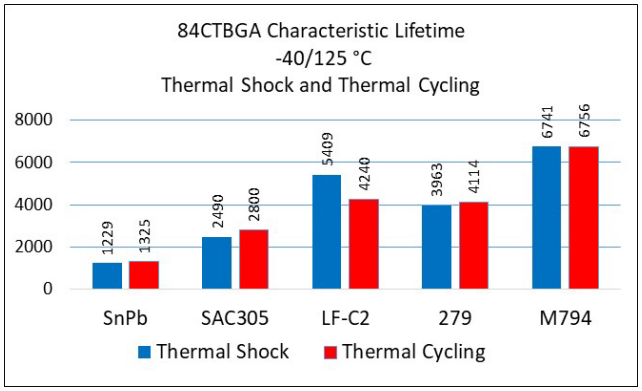


Figure 6. A bar chart comparing the characteristic lifetimes in **thermal shock** and **thermal cycling** for all alloys with the 84CTBGA component.

Table 5. A comparison of the Weibull statistics for the 192CABGA in thermal cycling and thermal shock.

192CABGA Thermal Cycling -40/125 °C				
Solder Alloy	Characteristic Lifetime η (cycles)	1% Failure (cycles)	Slope β	Correlation Coefficient, r^2
SnPb	1267	847	11.4	0.98
SAC305	1320	341	3.4	0.95
LF-C2	1966	1352	12.3	0.93
Indalloy 279	2758	1693	9.4	0.98
M794	2871	1948	11.9	0.98
192CABGA Thermal Shock -40/125 °C				
Solder Alloy	Characteristic Lifetime η (cycles)	1% Failure (cycles)	Slope β	Correlation Coefficient, r^2
SnPb	1208	925	17.2	0.93
SAC305	1299	361	3.6	0.91
LF-C2	2080	1224	8.7	0.94
Indalloy 279	2552	1803	13.3	0.95
M794	2645	1753	11.2	0.95

Table 6. A comparison of the Weibull statistics for the 84CTBGA in thermal cycling and thermal shock.

84CTBGA Thermal Cycling -40/125 °C				
Solder Alloy	Characteristic Lifetime η (cycles)	1% Failure (cycles)	Slope β	Correlation Coefficient, r^2
SnPb	1325	1059	20.5	0.86
SAC305	2800	1363	6.4	0.88
LF-C2	4240	1577	4.7	0.98
Indalloy 279	4114	1844	5.7	0.95
M794	6756	1468	3.0	0.97
84CTBGA Thermal Shock -40/125 °C				
Solder Alloy	Characteristic Lifetime η (cycles)	1% Failure (cycles)	Slope β	Correlation Coefficient, r^2
SnPb	1229	895	14.5	0.92
SAC305	2490	1772	12.5	0.93
LF-C2	5409	1320	3.3	0.92
Indalloy 279	3963	1853	6.1	0.99
M794	6741	1936	3.7	0.97

These data also show there are minimal differences in reliability between thermal shock and thermal cycling, based on either characteristic lifetime or 1% cumulative failure, which was not anticipated. The bar charts in Figure 5 and Figure 6 show only two cases where there is more than a 10 % difference in characteristic lifetime between cycling and shock, the 84CTBGA with SAC305 (12%) and the 84CTBGA with LF-C2 (28%). The Weibull plots in Appendix A compare thermal cycling and thermal shock for each alloy with 90% confidence limits overlaid. These plots show the statistical separations between cycling and shock are negligible, even with 28% difference in the characteristic lifetimes for the 84CTBGA with the LF-C2 alloy.

Table 5 and Table 6 show there are variations in Weibull slope (β) and correlation coefficient (r^2) across the data sets. Such variations are not unusual for this type of board level interconnect reliability test, even when only a single failure mode occurs. There are intrinsic, empirical noise factors that cannot be controlled or quantified that cause variability in the output. Sources of variability include component and printed circuit board fabrication, surface mount assembly of the test boards, solder alloy composition and microstructure, and thermal profile consistency across multiple test boards throughout the large volume of the test chamber.

Because of the obvious relationship between β and the characteristic lifetime and 1% cumulative failure, the variations in β must be acknowledged before drawing conclusions about reliability differences based on characteristic lifetime or 1% cumulative failure. Figure 7 shows that the 84CTBGA with the LF-C2 alloy performs much better in thermal shock based on characteristic lifetime but better in thermal cycling based on 1 % cumulative failure. That trend is reversed for SAC305. However, when the Weibull plots for LF-C2 and SAC305 with the 84CTBGA and 90% confidence limits (Appendix A) are considered, there are no statistically significant differences, which is consistent with the other data sets in the investigation. Thus,

in terms of the Weibull analysis, the results effectively are the same in thermal shock and thermal cycling.

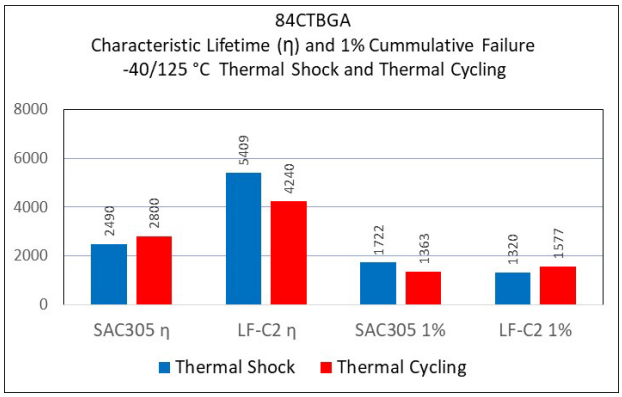


Figure 7. A bar chart comparing reliability based on characteristic lifetimes or 1% cumulative failure in **thermal shock** and **thermal cycling** for SAC305 and LF-C2 with the 84CTBGA component.

Failure Mode Analysis

SAC305 and SnPb Performance Baselines

Thermal fatigue is the expected wear-out mechanism for solder attachments in accelerated temperature cycling of electronic assemblies [1]. Both BGA components with SAC305 and eutectic SnPb attachments failed exclusively by thermal fatigue in the solder in both thermal cycling and thermal shock. Examples of thermal fatigue failures in SAC305 and SnPb are shown in Figure 8. The failure modes for SAC305 and SnPb under -40/125 °C thermal shock and thermal cycling conditions are the same failure modes observed under ten milder thermal cycling profiles with lower ramp rates of about 10 °C/minute in the iNEMI Alternate Alloys Project [26-33].

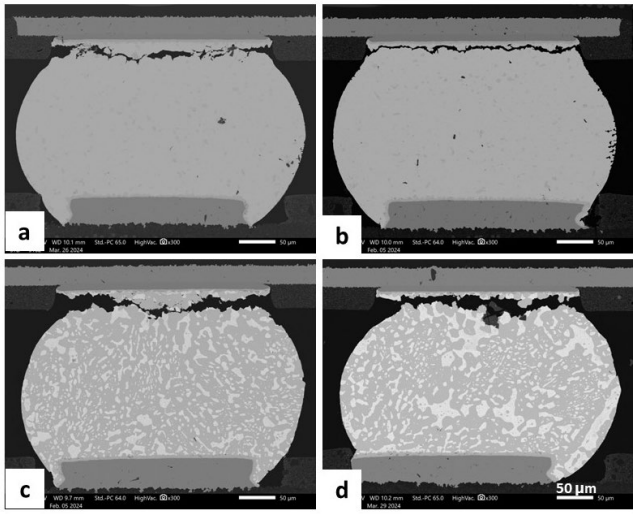


Figure 8. Solder joint thermal fatigue failures in SAC305 (a and b) and eutectic SnPb (c and d). The crack propagation path is through the bulk solder, but it can be close to the intermetallic layer (b and d).

When SAC305 and eutectic SnPb ball grid arrays are exposed to temperature cycling, the solders undergo significant microstructural evolution due to the combined effects of strain and temperature in the strain-localized region at the package side of the BGA solder joint. The processes of microstructural evolution are different for the two alloys, but thermal fatigue cracks initiate and propagate to failure through the strain-localized regions of both solders. The crack propagation path may be close to the IMC interfacial layer, but it is still within the bulk solder.

During solidification of SAC solders, the Ag and Sn react to form networks of Ag_3Sn intermetallic precipitates at the primary Sn dendrite boundaries. These precipitates are the primary strengthening mechanism in SAC solders [34, 35]. As the Ag_3Sn precipitates coarsen during temperature cycling, they become less effective in inhibiting dislocation movement and slowing damage accumulation. Coarsening of the Ag_3Sn precipitates is followed by local recrystallization, global recrystallization, crack propagation along the newly formed Sn boundaries with crack branching, and cavitation at boundary triple points. This pattern of microstructural evolution is characteristic of the thermal fatigue failure process in the SAC alloys [36]. Figure 9a is a higher magnification backscattered electron image that illustrates fatigue cracking and Ag_3Sn precipitate coarsening in SAC305 solder. There are only a few larger, coarsened Ag_3Sn precipitates in the vicinity of the fatigue crack, in contrast to an abundance of smaller precipitates below the strain-localized region of crack propagation.

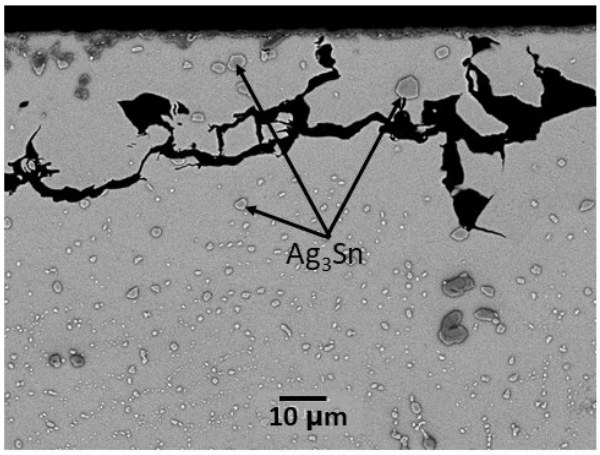


Figure 9. Thermal fatigue cracking and precipitate coarsening in a SAC305 solder joint.

The as-solidified SnPb microstructure consists of Sn-rich and Pb-rich phases. During temperature cycling, the SnPb microstructure evolves by a process called phase coarsening, which is grain growth under the combined effects of strain and temperature in the strain-localized region [37]. Phase coarsening in SnPb solder is analogous to precipitate coarsening in SAC solder. Figure 10 is a higher magnification backscattered electron image that illustrates fatigue cracking and phase coarsening in a SnPb solder joint. Only larger Pb-rich particles (white phase) are found in the vicinity of the fatigue crack due to phase coarsening, while numerous smaller Pb-rich particles are found below the strain-localized

region of crack propagation. In SnPb solder, the crack propagation path is mostly between the Sn-rich and Pb-rich phases.

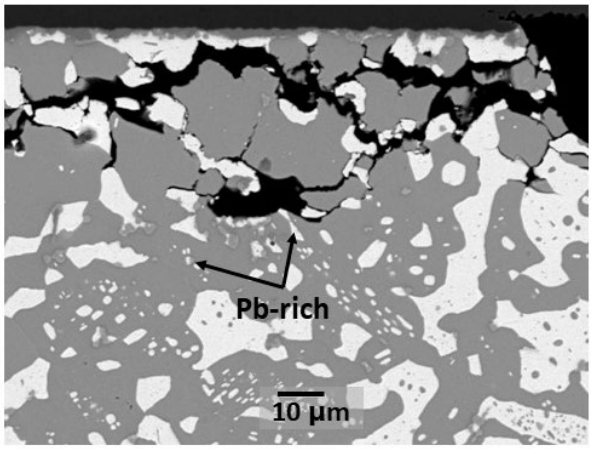


Figure 10. Thermal fatigue cracking and phase coarsening in a SnPb solder joint.

High-Performance Alloys

The results from earlier thermal cycling studies using high-performance alloys and the same BGA test vehicles from the current study, showed that thermal fatigue in the bulk solder was the predominant failure mode. However, interfacial fracturing and mixed mode failures also were detected in addition to bulk solder fatigue failures, particularly with aggressive thermal profiles such as -40/125 °C and -55/125 °C [16-19]. Often, multiple failure modes were detected within the same test cell.

The high-performance alloy results from the current thermal shock study are consistent with the earlier work. While solder fatigue was the predominant failure mode, interfacial fracturing and mixed mode failures also were detected with both thermal cycling and thermal shock profiles. The scanning electron micrographs in Figure 11 illustrate the three failure modes. Table 7 shows the failure modes found with each high-performance alloy in thermal cycling and thermal shock.

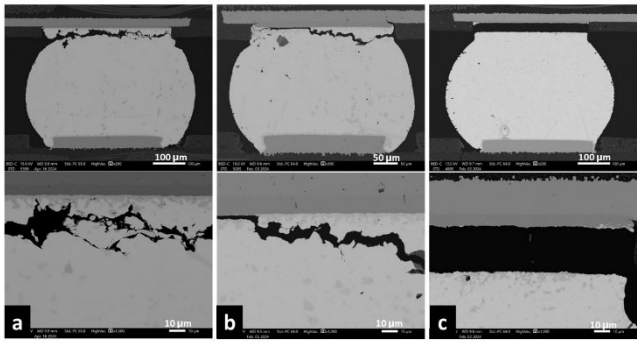


Figure 11. Failure modes in high-performance alloy solder joints resulting from thermal cycling or thermal shock testing: a) complete thermal fatigue, b) mixed mode, fatigue and interfacial and c) complete interfacial cracking.

Table 7. Failure modes for each alloy in thermal cycling and thermal shock.

Solder Alloy	Thermal Cycling			Thermal Shock		
	Solder Fatigue	Mixed Mode	Interfacial	Solder Fatigue	Mixed Mode	Interfacial
SAC305	X			X		
SnPb	X			X		
M794	X	X	X	X	X	X
Indalloy 279	X	X		X	X	
LF-C2	X	X	X	X	X	X

DISCUSSION

Solder fatigue was the predominant failure mode in this study, but interfacial cracking also was detected with thermal cycling and thermal shock profiles and the three high-performance solder alloys. The type of interfacial cracking in this study propagates along the boundary between the intermetallic (IMC) layer and the BGA pad. It has been suggested that interfacial cracking or fracturing occurs if the strength of a solder is sufficient to resist fatigue, resulting in the cyclic stresses being transferred to a lower strength soldered interface [38]. Interfacial failures of soldered interconnects normally are associated with the early failure period of the failure rate curve ("bathtub" curve [39]). Mixed mode crack propagation, a combination of thermal fatigue and interfacial cracking in the same interconnect, also was reported.

Multiple failure modes can manifest as bends in a Weibull plot and poor fit to the curve. However, in previous high-performance alloy studies, there was no evidence of true early life failures in the Weibull plots, and the occurrence of multiple failure modes did not always have an obvious effect on the Weibull statistics [16]. The current findings are consistent with those earlier results in that the presence of multiple failure modes does not have a noticeable effect on the Weibull statistics. It also is important to note that there was no evidence of interfacial cracking at time zero in any of the baseline samples, so interfacial cracking cannot be attributed to assembly quality defects.

Although there is not complete agreement in the literature, the results from many investigations show that failures occur faster in thermal shock than in thermal cycling. This trend is consistent with the hypothesis that the faster ramp rates associated with thermal shock testing produce larger creep strain energy densities, hence more damage in the solder joints leading to fewer cycles to failure [40]. That certainly is not the case with the current comparison of thermal cycling to thermal shock, where the performance in cycling and shock are indistinguishable despite a substantial difference in ramp rate. It would be difficult to consider these current findings anomalous or spurious since they are consistent for two BGA components, the SAC305 and SnPb performance baseline alloys, and three high-performance solder alloys of quite different compositions.

The IPC-9701B standard for thermal cycling specifies a maximum ramp rate of 20 °C/minute to avoid a thermal shock condition that can accelerate failure modes other than the desired low cycle fatigue failure mode in the bulk solder. The hot and cold thermal shock ramp rates in this investigation were 68 °C/minute and 45 °C/minute respectively (Figure 3 and Table 4), which is two to three times the specified maximum. Although the ramp rate was much higher in shock than cycling, the widely deployed performance baseline alloys, eutectic SnPb and SAC305, failed exclusively by solder fatigue. The failures for the high-performance alloys in cycling and shock are not exclusively by thermal fatigue and include mixed mode and interfacial failures.

The same types of non-solder fatigue failures were reported in tests of identical BGA components and alloys using ramp rates of only 10 °C/minute [16-19]. The presence of multiple failure modes in thermal shock and thermal cycling has minimal effect on the Weibull statistics, which also is consistent with previous results using the ramp rate of 10 °C/minute. Despite a much higher ramp rate, the failure modes in thermal shock were the same as in thermal cycling and produced the same results quantitatively. These findings were consistent with both BGA components and the five solder alloys used in the study. For these test conditions, components, and solder alloys, the same results were achieved in thermal shock compared to thermal cycling with a 30% savings in test duration.

SUMMARY

Accelerated temperature cycling was used to evaluate the thermal fatigue performance (reliability) of solder interconnects in electronic assemblies. A review of the literature showed that increasing the ramp rate can decrease the cycles to failure significantly. In turn, this can shorten test times, reduce qualification cycles, and accelerate product development. However, fast ramp rates associated with thermal shock testing are not recommended typically because of the risk for accelerating failures other than the desired low cycle fatigue failure mode in the bulk solder.

This investigation was conducted to compare board level interconnect reliability and failure mode using test conditions representative of thermal cycling and thermal shock. The accelerated temperature profile was -40 °C to 125 °C with the cycling ramp rates approximately three times faster with thermal shock and with equal dwell times in cycling and shock. The test matrix was comprised of two ball grid array (BGA) test vehicles fabricated with five different solder alloys. The alloys included eutectic SnPb and SAC305 as performance baselines and three high-performance SAC-based alloys modified with additions of antimony (Sb) or bismuth (Bi).

Despite a significant disparity in ramp rate, there was an insignificant difference in reliability between thermal shock and thermal cycling. Reliability was quantified based on characteristic lifetime and 1% cumulative failure from on a 2-parameter Weibull analysis. These reliability findings were applicable to the five solder alloys and two BGA components.

The fast ramp rate in the thermal shock test generated the same fatigue failures in SnPb and SAC305 solder attachments as the slower ramp rate in the thermal cycling test. Thus, the reliability measured in thermal shock matched the reliability in thermal cycling and did so without altering the solder fatigue failure mode of SnPb or SAC305 solder attachments.

Solder fatigue was the predominant failure mode for the three high-performance alloys, but these alloys also showed susceptibility to interfacial and mixed mode failures in thermal cycling and thermal shock. These failure modes were not considered to be anomalous because they were reported in a previous study using these BGA components and alloys when tested with a ramp rate of only 10 °C/minute. Regardless of the occurrence of multiple failure modes with the high-performance alloys, the reliability measured in thermal shock matched the reliability in thermal cycling.

In conclusion, for these specific test conditions, components, and solder alloys, the same results were achieved in thermal shock compared to thermal cycling. In this investigation, a 30% savings in test duration was achieved in thermal shock due to faster ramp rates that shortened the cycle time compared to thermal cycling. This resulted in the number of cycles to failure being effectively the same in shock and cycling for each test cell. The authors caution the reader that this level of test duration improvement may not be typical due to the influence that test characteristics such as component type, dwell time, ramp rate, and failure mode have on the solder joint integrity.

ACKNOWLEDMENTS

The authors thank the staffs at iNEMI and the HDP User Group, especially Grace O'Malley, Shekhar Chandrashekhar, and Larry Marcanti for their help in establishing and nurturing the collaborative agreement and for their continued support in coordinating the work between the cooperating consortia. Many thanks to Michael Meilunas of Universal Instruments for performing the thermal cycling and thermal shock tests, and Dave Vicari, Director of the Advanced Process Lab at Universal Instruments and Jim Wilcox, Director of the Universal AREA Consortium for project support. The Project Team also thanks Jim Fuller of Sanmina and Tony Senese of Panasonic for PCB test vehicle fabrication and support. The authors also express gratitude to their respective companies that have supported the various phases of the iNEMI Alloy Project to evaluate alternative Pb-free solder alloys for over a decade including the current collaborative Phase 4 program between iNEMI and HDP that is exploring high-performance Pb-free solder alloys.

REFERENCES

[1] IPC-9701B, "Thermal Cycling Test Method for Fatigue Life Characterization of Surface Mount Attachments," IPC, Bannockburn, IL, 2021.

[2] JEDEC JESD22-104F.01, “Temperature cycling,” JEDEC Solid State Technology Association, Arlington, VA, 2000, pp. 11.
[3] V. S. Sastry, J. C. Manock, and T. I. Ejim, “Effect of Thermal Cycling Ramp Rates on Solder Joint Fatigue Life,” *J. SMT*, January 2001, pp. 23-28.
[4] R. Ghaffarian, "Effect of thermal cycling ramp rate on CSP assembly reliability," *Proceedings. 51st Electronic Components and Technology Conference (Cat. No.01CH37220),* Orlando, FL, USA, 2001, pp. 1170-1174, doi: 10.1109/ECTC.2001.927974.
[5] S. Sahasrabudhe, E. Monroe, S. Tandon and M. Patel, "Understanding the effect of dwell time on fatigue life of packages using thermal shock and intrinsic material behavior," *Proceedings 53rd Electronic Components and Technology Conference*, New Orleans, LA, USA, 2003, pp. 898-904, doi: 10.1109/ECTC.2003.1216398.
[6] J.W.C. de Vries, M.Y. Jansen, W.D. van Driel, “On the difference between thermal cycling and thermal shock testing for board level reliability of soldered interconnections,” *Microelectronics Reliability*, 47, 2007, pp. 444-449. [7] Charlie J. Zhai, Sidharth, and Richard Blish II, “Board Level Solder Reliability Versus Ramp Rate and Dwell Time During Temperature Cycling,” *IEEE Transactions on Device and Materials Reliability,* IEEE Transactions on Device and Materials Reliability, vol. 3, no. 4, December 2003, pp. 207-212.
[8] Y. Qi, H. R. Ghorbani and J. K. Spelt, "Thermal Fatigue of SnPb and SAC Resistor Joints: Analysis of Stress-Strain as a Function of Cycle Parameters," in *IEEE Transactions on Advanced Packaging*, vol. 29, no. 4, pp. 690-700, Nov. 2006, doi: 10.1109/TADVP.2006.884805.
[9] Milos Dusek, Martin Wickham, and Christopher Hunt, “The Impact of Thermal Cycle Regime on the Shear Strength of Leadfree Solder Joints,” Soldering & Surface Mount Technology, vol 17, issue 22, 2005, https://doi.org/10.1108/09540910510597474
[10] Jussi Hokka, Toni T. Matilla, Hongbo Xu, and Mervi Paulasto-Kröckel, “Thermal Cycling Reliability of Sn-Ag-Cu Solder Interconnections. Part 1: Effects of Test Parameters,” Journal of Electronic Materials, vol. 42, no. 6, 2013, pp, 1171-1183, doi: 10.1007/s11664-013-2551-x
[11] Jussi Hokka, Toni T. Matilla, Hongbo Xu, and Mervi Paulasto-Kröckel, “Thermal Cycling Reliability of Sn-Ag-Cu Solder Interconnections - Part 2: Failure Mechanisms,” vol. 42, no. 6, 2013, pp. 963-972, doi: 10.1007/s11664-013-2475-5.
[12] Gunter Grossman and Ludger Weber, “Metallurgical considerations for accelerated testing of soft solder joints,” IEEE Transactions on Components, Packaging and Manufacturing Technology - Part C, vol. 20, no. 3, July 1997, pp. 213-218.
[13] Gregory Henshall, Jian Miremadi, Richard Parker, Richard Coyle, Joe Smetana, Jennifer Nguyen, Weiping Liu, Keith Sweatman, Keith Howell, Ranjit S. Pandher, Derek Daily, Mark Currie, Tae-Kyu Lee, Julie Silk, Bill Jones, Stephen Tisdale, Fay Hua, Michael Osterman, Bill Barthel, Thilo Sack, Polina Snugovsky, Ahmer Syed, Aileen Allen, Joelle Arnold, Donald Moore, Graver Chang, and Elizabeth Benedetto, “iNEMI Pb-Free Alloy Characterization Project Report: Part I – Program Goals, Experimental Structure, Alloy Characterization, and Test Protocols for Accelerated Temperature Cycling,” *Proceedings of SMTAI 2012*, Orlando, FL, October, 2012, pp. 335-347.
[14] Amkor Technology Datasheets: CABGA DS550T (Rev. 11/15) and CTBGA DSS550N (Rev. 1/07), Amkor Technology, www.amkor.com, Tempe, AZ.
[15] Richard Coyle, Richard Parker, Keith Howell, Dave Hillman, Joe Smetana, Glen Thomas, Stuart Longgood, Michael Osterman, Eric Lundeen, Polina Snugovsky, Julie Silk, Andre Kleyner, Keith Sweatman, Rafael Padilla, Tomoyasu Yoshikawa, Jasbir Bath, Mitch Holtzer, Hongwen Zhang, Jerome Noiray, Frederic Dulondel, Raiyo Aspandiar, and Jim Wilcox, “A Collaborative Industrial Consortia Program for Characterizing Thermal Fatigue Reliability of Third-Generation Pb-Free Alloys,” *Proceedings of SMTAI 2016*, Rosemont, IL, September 2016, pp. 188-196.
[16] Richard Coyle, Charmaine Johnson, Dave Hillman, Tim Pearson, Michael Osterman, Joe Smetana, Keith Howell, Hongwen Zhang, Julie Silk, Jie Geng, Derek Daily, Babak Arfaei, Ranjit Pandher, Andre Delhaise, Stuart Longgood, and Andre Kleyner, “Enhancing Thermal Fatigue Reliability of Pb-Free Solder Alloys with Additions of Bismuth and Antimony,” *Proceedings of SMTAI 2020 Virtual*, September 28 - October 23, 2020, pp. 339-354.
[17] Richard Coyle, Charmaine Johnson, Dave Hillman, Richard Parker, Michael Osterman, Joe Smetana, Tim Pearson, Babak Arfaei, Keith Howell, Stuart Longgood, Andre Kleyner, Julie Silk, Andre Delhaise, Hongwen Zhang, Jie Geng, Ranjit Pandher, and Eric Lundeen, “Thermal Cycling Reliability and Failure Mode of Two Ball Grid Array packages with High Reliability Pb-Free Solder Alloys,” *Proceedings of SMTAI*, Rosemont, IL, September 2019, pp. 439-456.
[18] Richard Coyle, Dave Hillman, Richard Parker, Charmaine Johnson, Michael Osterman, Jasbir Bath, Babak Arfaei, Andre Delhaise, Keith Howell, Brook Sandy-Smith, Joe Smetana, Stuart Longgood, “The Effect of Bismuth, Antimony, or Indium on the Thermal Fatigue of High Reliability Pb-Free Solder Alloys,” *Proceedings of SMTAI*, Rosemont, IL, October 2018.
[19] Richard Coyle, Dave Hillman, Charmaine Johnson, Richard Parker, Brook Sandy-Smith, Hongwen Zhang, Jie Geng, Michael Osterman, Babak Arfaei, Andre Delhaise, Keith Howell, Jasbir Bath, Joe Smetana, Stuart Longgood, Andre Kleyner, Julie Silk, Ranjit Pandher, Eric Lundeen, and Jerome Noiray “Alloy Composition and Thermal Fatigue of High Reliability Pb-Free Solder Alloys,” *Proceedings of SMTAI*, Rosemont, IL, October 2018.
[20] W. Engelmaier, “The use environments of electronic assemblies and their impact on surface mount solder attachment reliability,” *IEEE Trans. Components, Hybrids, and Manufacturing Technology,* vol. 13, no.4, December 1990, pp. 903-908.
[21] Richard Coyle, Dave Hillman, Tim Pearson, Michael Osterman, Joe Smetana, Keith Howell, Julie Silk, Hongwen Zhang, Jie Geng, Derek Daily, Anna Lifton, Morgana Ribas, Raiyo Aspandiar, Faramarz Hadian, Chloe Feng, Ranjit

Pandher, Jayse McLean, James Wertin, Babak Arfaei, Jean-Christophe Riou, Madan Jagernauth, Denny Fritz, Shantanu Joshi, Jasbir Bath, Stuart Longgood, and Andre Kleyner, "A Collaborative Consortia Project to Assess the Effect of Thermal Cycling Dwell Time on the Reliability of High-Performance Solder Alloys," *Proceedings of SMTAI International*, October 9-12, Minneapolis, MN, 2023, pp. 158-183.

[22] Tim Pearson, Richard Coyle, Michael Osterman, Faramarz Hadian, Dave Hillman, Charmaine Johnson, Jeffrey Chumbley, Xinzhi Feng, Joe Smetana, Keith Howell, Julie Silk, Babak Arfaei, Hongwen Zhang, Jie Geng, Derek Daily, Ranjit Pandher, Shantanu Joshi, Stuart Longgood, and Andre Kleyner, "Thermal Fatigue Reliability of a 1206 Chip Resistor with High-Performance Pb-Free Solder Alloys," *Proceedings of SMTAI International*, Minneapolis, MN, October 31- November 3, 2022, pp. 341-358.

[23] S.A. Belyakov, B. Arfaei, C. Johnson, K. Howell, R. Coyle, and C.M. Gourlay, "Phase Formation and Solid Solubility in High Reliability Pb-free Solders Containing Bi, Sb or In," *Proceedings of SMTA International*, Rosemont, IL., September 22-26, 2019, pp. 492-506,

[24] S.A. Belyakov, K. Sweatman, T. Akaiwa, T. Nishimura and C.M. Gourlay, "Precipitation of Bi and SbSn Phases in Next-Generation Pb-Free Solders," *Proceedings of SMTA International*, Rosemont, IL., September 22-26, 2019, pp. 481-491.

[25] S.A. Belyakov, R.J. Coyle, B. Arfaei,3,4 J.W. Xian, and C.M. Gourlay, "Microstructure and Damage Evolution During Thermal Cycling of Sn-Ag-Cu Solders Containing Antimony," *Journal of Electronic Materials*, Vol. 50, No. 3, 2021. https://doi.org/10.1007/s11664-020-08507-x

[26] Richard Coyle, Richard Parker, Joseph Smetana, Elizabeth Benedetto, Keith Howell, Keith Sweatman, Weiping Liu, Michael Osterman, Julie Silk, Aileen Allen, Mitch Holtzer, Rafael Padilla, and Tomoyasu Yoshikawa "iNEMI Pb-Free Alloy Characterization Project Report: PART IX – Summary of the Effect of Isothermal Preconditioning on Thermal Fatigue Life," *Proceedings of SMTAI 2015*, Chicago, IL, September 27 –October 1, 2015, pp. 743-755.

[27] Richard Coyle, Richard Parker, Elizabeth Benedetto, Keith Howell, Keith Sweatman, Stuart Longgood, Joseph Smetana, Aileen Allen, Peter Read, Babak Arfaei, and Francis Mutuku, "iNEMI Pb-Free Alloy Characterization Project Report: PART VIII - Thermal Fatigue Results for High-Ag Alloys at Extended Dwell Times," *Proceedings of SMTAI 2014*, Chicago, IL, October 2014, pp. 547-560.

[28] Keith Sweatman, Richard Coyle, Richard Parker, Keith Howell, Elizabeth Benedetto, Joseph Smetana, Aileen Allen, Weiping Lui, Julie Silk, "iNEMI Pb-Free Alloy Characterization Project Report: PART VII - Thermal Fatigue Results for Low-Ag Alloys at Extended Dwell Times," *Proceedings of SMTAI 2014*, Chicago, IL, October 2014, pp. 561-574.

[29] Richard Coyle, Richard Parker, Babak Arfaei, Francis Mutuku, Keith Sweatman, Keith Howell, Stuart Longgood, and Elizabeth Benedetto, The Effect of Nickel Microalloying on Thermal Fatigue Reliability and Microstructure of SAC105 and SAC205 Solders, *Proceedings of Electronic Components Technology Conference*, IEEE, Orlando, FL, 2014, pp. 425-440.

[30] Richard Coyle, Richard Parker, Michael Osterman, Stuart Longgood, Keith Sweatman, Elizabeth Benedetto, Aileen Allen, Elviz George, Joseph Smetana, Keith Howell, and Joelle Arnold, "iNEMI Pb-Free Alloy Characterization Project Report: Part V – The Effect of Dwell Time on Thermal Fatigue Reliability," *Proceedings of SMTAI 2013*, Ft. Worth, TX, October 2013, pp. 470-489.

[31] Richard Coyle, Richard Parker, Babak Arfaei, Keith Sweatman, Keith Howell, Stuart Longgood, and Elizabeth Benedetto, "iNEMI Pb-Free Alloy Characterization Project Report: Part VI – The Effect of Component Surface Finish and Solder Paste Composition on Thermal Fatigue of SN100C Solder Balls," *Proceedings of SMTAI 2013*, Ft. Worth, TX, October 2013, pp. 490-414.

[32] Richard Parker, Richard Coyle, Gregory Henshall, Joe Smetana, and Elizabeth Benedetto, "iNEMI Pb-Free Alloy Characterization Project Report: Part II – Thermal Fatigue Results for Two Common Temperature Cycles," *Proceedings of SMTAI 2012*, Orlando, FL, October 2012, pp. 348-358.

[33] Richard Coyle, Richard Parker, Gregory Henshall, Michael Osterman, Joe Smetana, Elizabeth Benedetto, Donald Moore, Graver Chang, Joelle Arnold, and Tae-Kyu Lee, "iNEMI Pb-Free Alloy Characterization Project Report: Part IV - Effect of Isothermal Preconditioning on Thermal Fatigue Life," *Proceedings of SMTAI 2012*, Orlando, FL, October 2012, pp. 376-389.

[34] Richard Coyle, John Osenbach, Maurice Collins, Heather McCormick, Peter Read, Debra Fleming, Richard Popowich, Jeff Punch, Michael Reid, and Steven Kummerl, "Phenomenological Study of the Effect of Microstructural Evolution on the Thermal Fatigue Resistance of Pb-Free Solder Joints," *IEEE Trans. CPMT*, Vol. 1, No. 10, October 2011, pp. 1583-1593.

[35] Richard Coyle, Heather McCormick, John Osenbach, Peter Read, Richard Popowich, Debra Fleming, and John Manock, "Pb-free Alloy Silver Content and Thermal Fatigue Reliability of a Large Plastic Ball Grid Array (PBGA) Package," *Journal of SMT*, Vol. 24, Issue 1, January-March 2011, pp. 27-33.

[36] S. Dunford, S. Canumalla, and P. Viswanadham, "Intermetallic Morphology and Damage Evolution Under Thermomechanical Fatigue of Lead (Pb)-Free Solder Interconnections," *Proceedings of Electronic Components Technology Conference,* Las Vegas, NV, June 1-4, 2004, pp. 726-736.

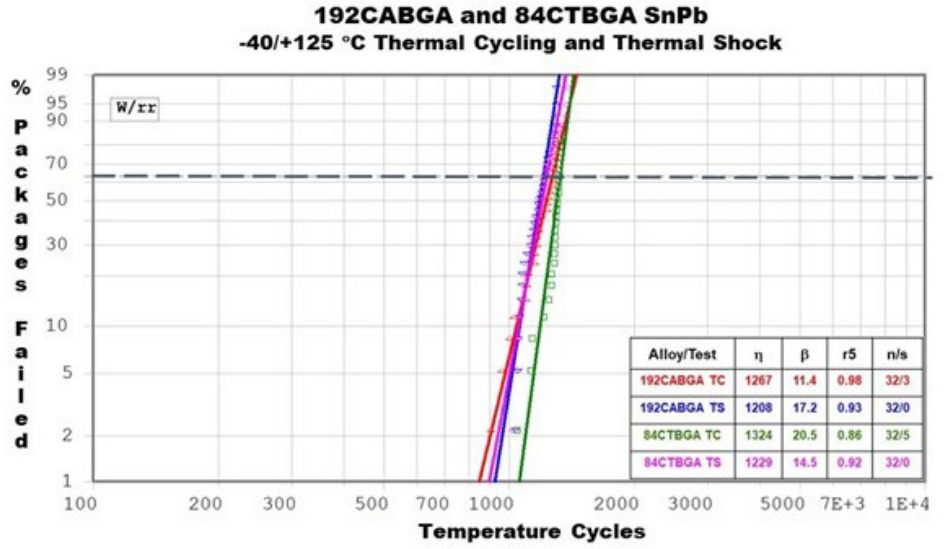
[37] John Manock, Richard Coyle, Brian Vaccaro, Heather McCormick, Richard Popowich, Debra Fleming, Peter Read, John Osenbach, and Dan Gerlach, "Effect of Temperature Cycling Parameters on the Solder Joint Reliability of a Pb-free PBGA Package," *Proceedings SMTAI 2007*, Orlando, FL, October 2007, pp. 564-573.

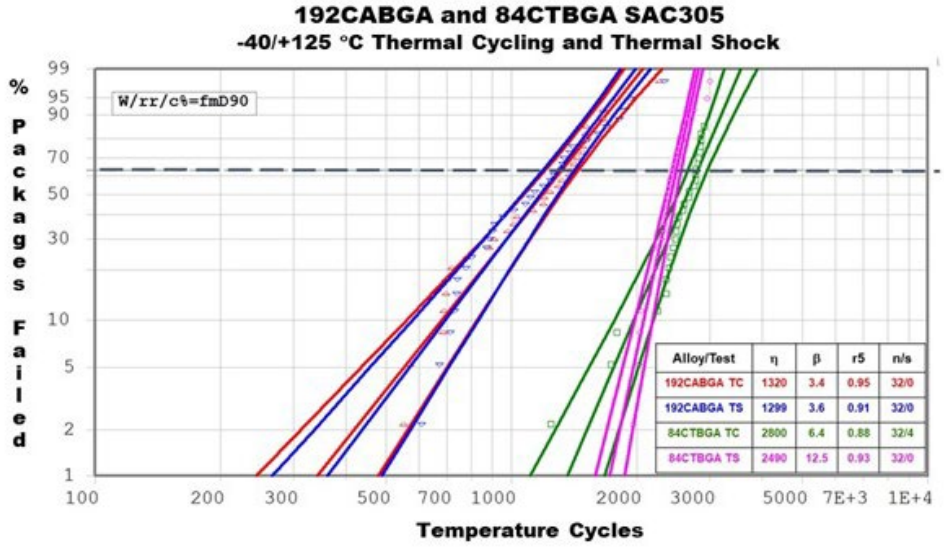
[38] Faramarz Hadian, Richard Coyle, Martin Anselm, Eric Cotts, Richard Popowich, Xinzhi Feng, and Lenora Clark, "The Thermal Cycling Performance of Hybrid Low Temperature Solder Joints Assembled at Different Peak

Reflow Temperatures," *Proceedings of SMTA International,* Minneapolis, MN, October 2022, pp. 529-548.
[39] *NIST/SEMATECH e-Handbook of Statistical Methods*, http://www.itl.nist.gov/div898/handbook/, Section 8.1.2.4, "Bathtub" curve, 2012. https://doi.org/10.18434/M32189
[40] John Lau and Walter Dauksher, "Effects of Ramp-Time on the Thermal-Fatigue Life of SnAgCu Lead-Free Solder Joints," *Proceedings of Electronic Components Technology Conference,* Lake Buena Vista, FL, May 31 - June 3, 2005, pp. 1292-1298.

.

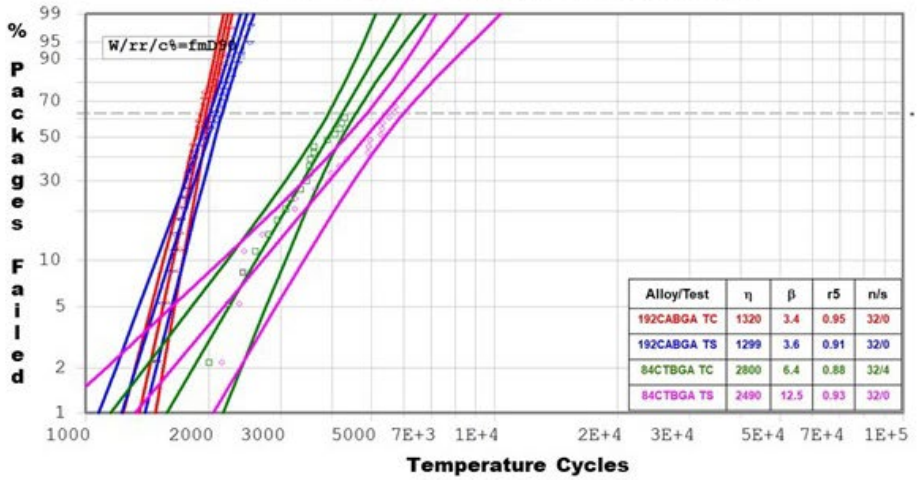
Appendix A
Weibull Plots SnPb and SAC305
-40/125 °C Thermal Cycling and Thermal Shock





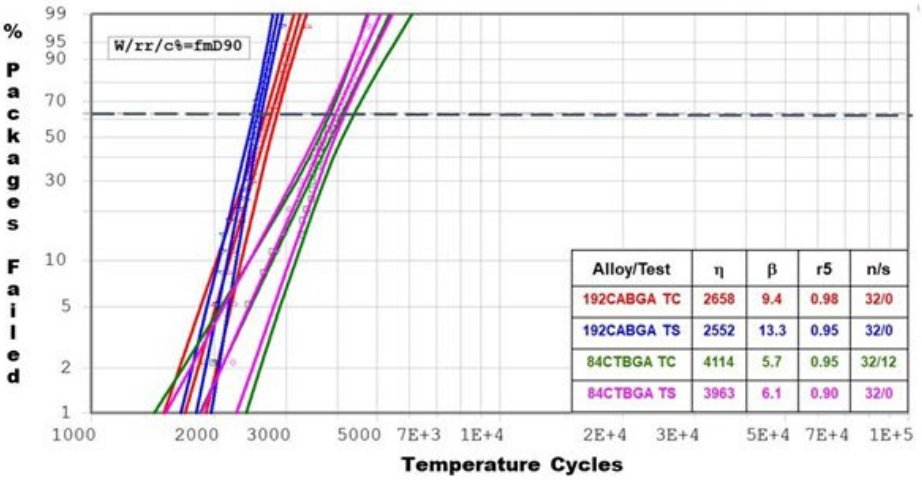
Appendix A
Weibull Plots LF-C2, 279 and 794
-40/125 °C Thermal Cycling and Thermal Shock

192CABGA and 84CTBGA LF-C2
-40/+125 °C Thermal Cycling and Thermal Shock



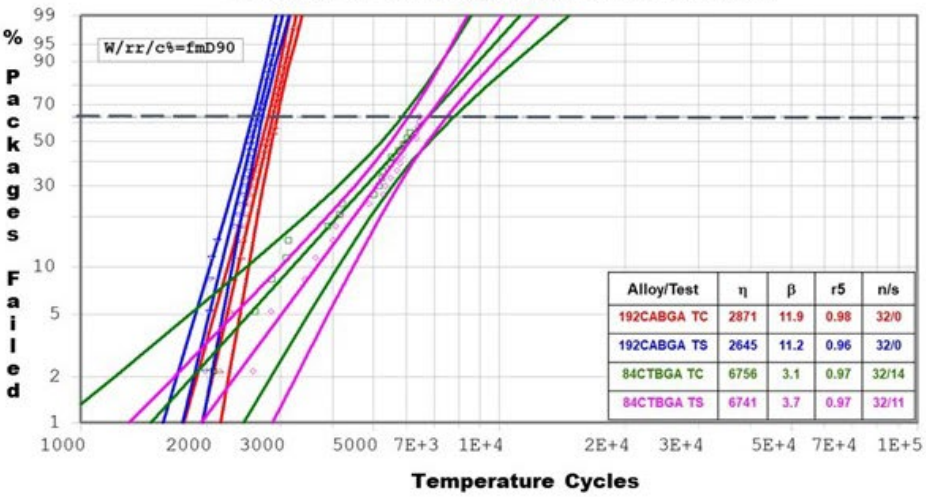
Alloy/Test	η	β	r5	n/s
192CABGA TC	1320	3.4	0.95	32/0
192CABGA TS	1299	3.6	0.91	32/0
84CTBGA TC	2800	6.4	0.88	32/4
84CTBGA TS	2490	12.5	0.93	32/0

192CABGA and 84CTBGA 279
-40/+125 °C Thermal Cycling and Thermal Shock



Alloy/Test	η	β	r5	n/s
192CABGA TC	2658	9.4	0.98	32/0
192CABGA TS	2552	13.3	0.95	32/0
84CTBGA TC	4114	5.7	0.95	32/12
84CTBGA TS	3963	6.1	0.90	32/0

192CABGA and 84CTBGA 794
-40/+125 °C Thermal Cycling and Thermal Shock



Alloy/Test	η	β	r5	n/s
192CABGA TC	2871	11.9	0.98	32/0
192CABGA TS	2645	11.2	0.96	32/0
84CTBGA TC	6756	3.1	0.97	32/14
84CTBGA TS	6741	3.7	0.97	32/11