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Case Study: Analyzing 0402 Capacitor Defects With Stencil Printing Misalignment When Using Water Soluble and No-clean Solder Pastes: Part 2

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ABSTRACT
This study investigated the cause of tombstoning for 0402 capacitors in surface mount technology (SMT). It serves as a follow-up investigation to the study conducted by Feng in SMTAI 2022 and sought to determine the cause of the high occurrence of tombstoning seen in Sample Group 4, even though the printing quality fell within the standards set by IPC-7527. Statistical analysis methods were used to determine if there was any significant difference between the target experimental printing offset and the additional SPI measured offset of the printed solder paste. Additional analysis was conducted to determine if there was a difference in solder paste accuracy between components that showed defects vs. those that did not. Finally, two test boards were subjected to reflow while oriented 90˚ counterclockwise to the original design to check the effects of changing the offset orientation of the solder paste. The analysis did reveal a significant difference in actual paste position from the target. However, the difference in the solder paste's measured positions did not show any correlation to defects. This study further indicates that reflow orientation can lead to even more defects depending on the direction of the paste offset.

INTRODUCTION
The rapid and continuous improvements in technology over the last few decades has revolutionized the way that all electronics are manufactured. Ever-increasing demand has forced innovative solutions to speed up production and the miniaturization of devices, leading to products can be smaller than ever. But these innovations have brought along new challenges in production that leave components more vulnerable to defects than ever before.

For example, in a surface-mount assembly, capacitors are attached to a printed circuit board (PCB) by use of a reflow oven. By this method, two solder paste deposits are stencil printed at each terminal. When the PCB enters the reflow oven, the solder paste reflows then solidifies, holding each terminal of the component and establishing electrical continuity. Occasionally, however, the capacitor is not soldered properly; the solder at one end of the component may reflow at a different time than the opposite end, for instance. No matter the reason, it can result in the capacitor only being soldered on one end. This defect is known as tombstoning.

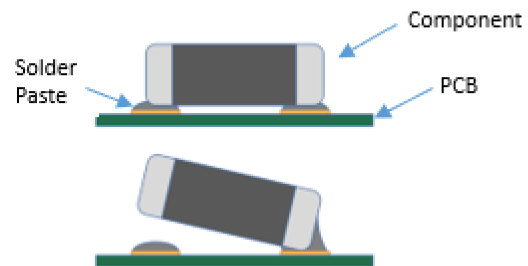


Figure 1: Tombstoning Defect

Tombstoning, specifically, is caused by the solder paste at both terminals failing to reflow at the same time, creating a wetting force at only one end of a component. Since these components are so small, the sudden force caused by the surface tension of the molten solder is significant enough to lift the component up so that it protrudes up off of the board. This is a major issue that creates an open circuit, stopping signals from being transmitted through that path, leaving the board nonfunctional.

Moreover, even a low occurrence of defects like these are compounded by the fact that many similar capacitor components can occupy a single board and the extremely high volumes at which these products are produced. This suggests that even a low rate of failure for an individual component can lead to a large proportion of products that are not functional.

Research Problem
An industry partner of Rochester Institute of Technology recently expressed concern that its 0402 capacitors displayed a concerningly high probability of tombstoning [1]. As previously stated, even a small occurrence of failure of components of this nature can lead to a major production deficiency. This led to a study, conducted by Feng in 2022, that analyzed several different factors in an attempt to identify the cause of failure and find a solution.

The results of one sample group in particular yielded an unexpectedly high number of defects, despite the fact that the tolerances fell within the acceptable standards set by IPC-A-610G. Additionally, defects were only observed in the components that were printed with a 90˚ orientation, while those printed with a 0˚ orientation yielded none. During the peer review of this study, it

came into question how precise the actual position of the solder paste was compared to the target experimental offset. This factor had not been scrutinized in the initial study but presented a possible cause for the anomalous results.

The conclusion of the report also acknowledged the anomalous results and, after some re-examination of the experimental method, remarked that it was likely due to the shape of the solder paste used, a bowtie shape, which was particularly sensitive to offsets in the Y-axis, while offset in the X-axis actually proved helpful in increasing solder contact during the soldering process. The bowtie shape of the solder paste is shown in Figure 2 and the effect of offsets in each direction can be seen in Figure 3.

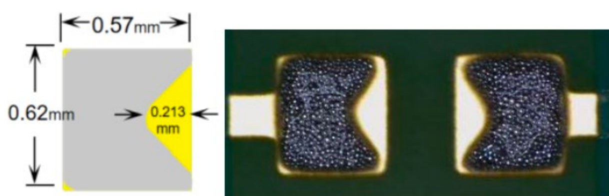


Figure 2: Bowtie Solder Paste Shape

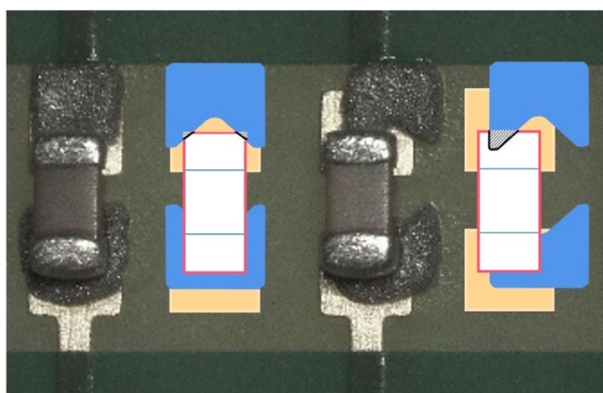


Figure 3: Effect of Offset in X & Y-Axis

This study will further analyze data from the 2022 study in order to verify the cause of the unexpected tombstoning trend that was observed and recommend ideal print configurations for manufacturers.

LITERATURE REVIEW

Electronic device miniaturization

Technology has come a long way within the last few decades. Electronic devices that used to require their own shelf can now fit into the palm of your hand and perform a multitude of additional functions at the same time. However, this has also led to brand new manufacturing challenges. The surface tension produced by molten solder is no longer an insignificant force and can actually lift these nominally 0.04x0.02 inch components off of the PCB, resulting in a tombstone defect. This defect is caused by solder paste at opposite ends of the components being heated for different lengths of time [2]. This issue can be mitigated if the solder alloy can be brought to a semi-molten state, thus maintaining an equal balance of force at each end of the component, but this is not always possible [2]. The risk and degree to which a component will tombstone is determined by the volume of the deposited solder, the geometry of the pad and any features the component or PCB design may have [1, 5].

Additionally, with components being so small, accuracy during product fabrication is critical to success. As such, any deficiencies in solder printing, device placement, reflow limitations or similar can result in limiting a solder joints fatigue life [1, 3]. If the misalignment is severe enough, it can result in an open solder joint from either tombstoning or nonwetting.

Manufactured components must comply with the standards set by IPC-7527. This standard lays out the acceptable quality criteria for all solder-based printing via visual evaluation, for the purpose of process optimization [6]. This criterion includes, but is not limited to, solder paste misalignment, area and height; slumping and adequate lighting.

Previous Study

A study conducted in conducted in 2022, by Feng, sought to identify the effect of misalignment of solder paste on the surface tension and wetting force attained during reflow. To achieve this, solder paste for components were printed at deliberately offset increments on each axis. As seen in Figure 4, components were offset in each combination 0%, 25% and 50% in each direction, as well as an additional group with a 37.5% offset in each direction to gauge the effect on the reflow process. Additionally, these offsets were tested with three different components and solder paste types, at both a 0˚ and 90˚ orientation to get a full scope of the effect.

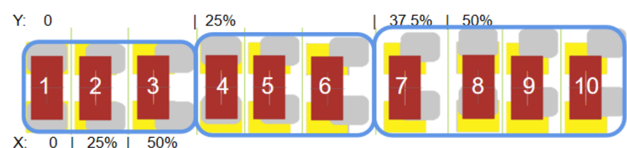


Figure 4: Sample Group Solder Paste Offsets

Additionally, the solder paste was printed in a 'bowtie' shape, as seen in Figure 2, as a means to artificially increase the occurrence of defects. The PCB would enter the reflow oven from the right side first, meaning that the reflow process would begin at the rightmost solder deposits on the PCB (refer to Figure 5) and gradually move leftward. A sample of the results of that study are shown in Figure 6.

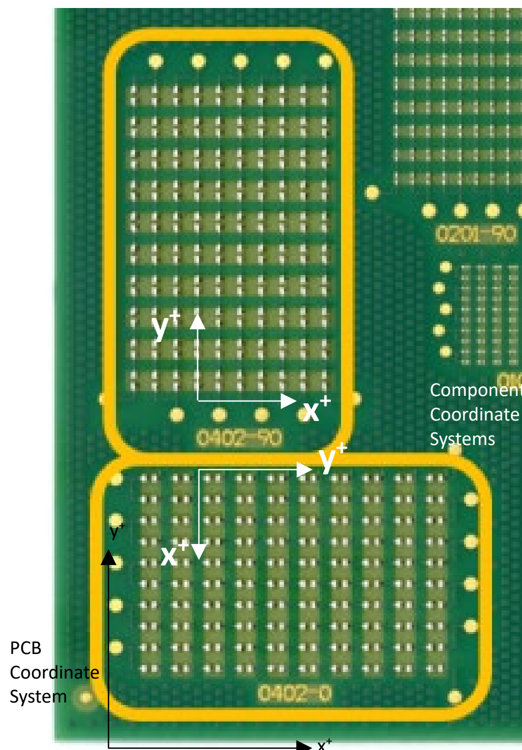


Figure 5: Component Locations & Configurations on PCB

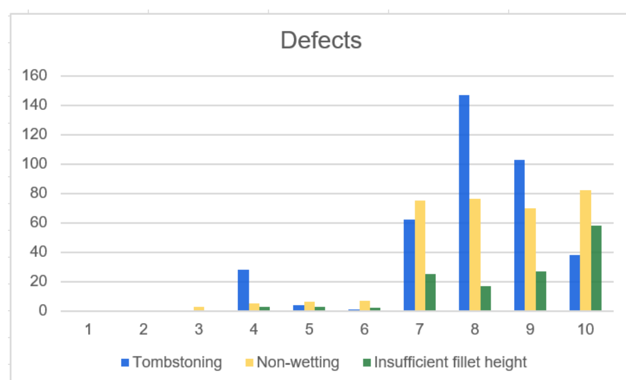


Figure 6: Defect Sum by Offset Test Group

As seen from Figure 6, and referencing Figure 4, the results are mostly what was expected. Components that went through the reflow process and were compliant with IPC-7527 experienced very low rates of failure, while those that did not comply with this standard showed very high failure rates. However, Sample Group 4 showed a tombstone rate that was more comparable to components that didn't meet the standard, even though there was no experimental parameter that should have led to this. The only theory was that the bowtie shape of the deposits had made the components more sensitive to offsets in the Y-direction.

METHODOLOGY

Objective and Structure

The objective of this study is to determine the cause of the unusually high number of tombstoning defects observed in the study conducted by Feng in 2022, beyond the original scope. Specifically, this project will investigate the accuracy of solder paste positioning and any potential methodology oversights employed in the previous study, rather than the different manufacturing conditions that were tested previously, in order to identify the cause of the high defect rate seen in Sample Group 4.

The study conducted by Feng identified three potential sources of variation: solder paste type, component type and print orientation. Additionally, the tested solder paste was deliberately shaped in a bowtie and positioned in offset increments in order to exaggerate the occurrence of defects seen during typical manufacturing and better identify trends that resulted from different conditions.

Sample Group 4, specifically, yielded far more defects than similar test groups. This is in spite of it falling within the IPC-A-610G standard, which provides a baseline for producing quality parts. Sample Group 4 is defined as containing all three component types and solder pastes at both a 0˚ and 90˚ print orientation, with a solder paste offset in the Y-axis of 25%.

To determine the actual accuracy of the solder paste printings, as series of one-sample t-tests were conducted. These tests indicated whether or not the tested solder paste offset significantly deviated from the experimental target in the X or Y-axis in both the 0˚ and 90˚ orientation, with a 95% level of confidence. Furthermore, two-sample t-tests were conducted to compare the positions of solder paste of components that tombstoned vs. those that did not.

Finally, two additional test boards were run with precisely the same experimental parameters that Group 4 had before, however, the board was sent through the reflow oven reoriented 90˚ counterclockwise. This resulted in the components that were positioned in the 0˚ orientation in the original experiment to now resemble the 90˚ oriented ones and the components that were originally soldered with a 90˚ orientation to resemble the components soldered at 0˚, but with offset in the opposite direction.

Normally when conducting data analysis of this nature, a normality test would also be run to verify that the collected data is useful. However, this was already done in the original study and doesn't need to be repeated here. Additionally, the original test data showed very little variation between solder paste types, so only one was used for this study.

RESULTS

Initial statistical analysis used one-sample t-tests to determine if the actual offset of the solder paste printed in Group 4 was significantly different from the target offset. An offset value of 0 would indicate exactly 25% offset in the component's Y-axis for both orientations. The results of these tests are shown below.

Figure 7 shows the distribution of offset error of each axis for the solder paste of each orientation, with respect

to the component. The t-test shown in Table 2 yielded a p-value that was greater than 0.05, meaning that there was no evidence to suggest that the X offset of the 0˚ oriented components was not what it should have been. However, every other t-test yielded a p-value that was less than 0.05, indicating that the offset was significantly different from the target. Looking at the averages calculated in each test, it is made clear that the Y offset was especially far from the experimental target: as much as 32 µm, as opposed to the 6µm seen from the X offset.

Figure 7: Solder Paste Error for All Components

Table 1: Group 4, 0˚ Orientation, X Offset One Sample t-Test

Null hypothesis: The average X offset of the solder paste of group 4 (0˚) is 0.	
Average	25.917
Std. Deviation	10.618
Count (n)	240
SEM	0.685
Deg. of Freedom	239
Predicted Offset	0
t-statistic	37.814
p-value	< 0.001

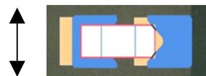


Table 2: Group 4, 0˚ Orientation, Y Offset One Sample t-Test

Null hypothesis:	The average Y offset of the solder paste of group 4 (0˚) is 0.
Average	0.888
Std. Deviation	15.283
Count (n)	240
SEM	0.986
Deg. of Freedom	239
Predicted Offset	0
t-statistic	0.900
p-value	0.369

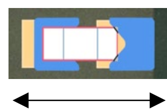


Table 3: Group 4, 90˚ Orientation, X Offset One Sample t-Test

Null hypothesis: The average X offset of the solder paste of group 4 (90˚) is 0.	
Average	-6.181
Std. Deviation	6.217
Count (n)	240
SEM	0.401
Deg. of Freedom	239
Predicted Offset	0
t-statistic	-15.402
p-value	<0.001

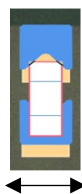
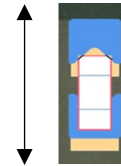


Table 4: Group 4, 90˚ Orientation, Y Offset One Sample t-Test

Null hypothesis:	The average Y offset of the solder paste of group 4 (90˚) is 0.
Average	32.047
Std. Deviation	17.083
Count (n)	240
SEM	1.103
Deg. of Freedom	239
Predicted Offset	0
t-statistic	29.062
p-value	<0.001



Two more one sample t-tests were performed to see if this deviation was present in the components that tombstoned. Once again, the following one sample t-tests (Tables 5 & 6) show a p-value less than 0.05, indicating that the deviation is present in the components that tombstoned. The calculated averages suggest the inaccuracy was slightly worse in the failed components, if only to a slight degree, as the average is higher than the previous net average.

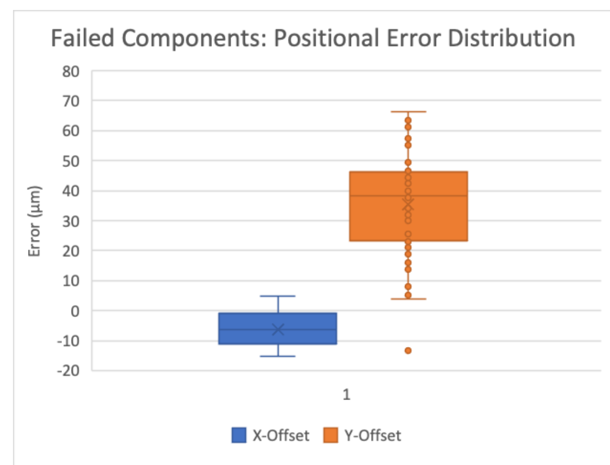


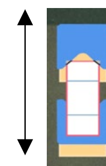
Figure 8: Solder Paste Error for Failed Components

Table 5: Group 4, Failed Components X Offset One Sample t-Test

Null hypothesis:	The average X offset of the failed components of group 4 (90˚) is 0.
Average	-6.182
Std. Deviation	5.826
Count (n)	60
SEM	0.752
Deg. of Freedom	59
Predicted Offset	0
t-statistic	-8.219
p-value	< 0.001

Table 6: Group 4, Failed Components Y Offset One Sample t-Test

Null hypothesis:	The average Y offset of the failed components of group 4 (90˚) is 0.
Average	35.408
Std. Deviation	16.669
Count (n)	60
SEM	2.152
Deg. of Freedom	59
Predicted Offset	0
t-statistic	16.454
p-value	< 0.001



These tests proved that the printed solder paste was not perfectly accurate, but not necessarily that it was the source of the failures observed. Now all that was left to do was prove the difference between the solder paste offset of the failed components and the successful ones.

To do this, the tombstoned components were compared to the entire sample in two-sample t-tests.

Table 7: X Offset, All Components vs. Failed Components, Two Sample t-Test

t-Test: Two-Sample Assuming Unequal Variances		
All components vs. failed components (X offset 90˚)		
	Variable 1	*Variable 2*
Mean	-6.181	-6.182
Variance	38.652	32.826
Observations	240	60
Hypothesized Mean Difference	0	
df	97	
t Stat	0.001	
P(T<=t) one-tail	0.500	
t Critical one-tail	1.661	
P(T<=t) two-tail	0.999	
t Critical two-tail	1.985	

Table 8: Y Offset, All Components vs. Failed Components, Two Sample t-Test

t-Test: Two-Sample Assuming Unequal Variances		
All components vs. failed components (Y offset 90˚)		
	Variable 1	*Variable 2*
Mean	32.047	35.408
Variance	291.821	279.780
Observations	240	60
Hypothesized Mean Difference	0	
df	92	
t Stat	-1.387	
P(T<=t) one-tail	0.084	
t Critical one-tail	1.662	
P(T<=t) two-tail	0.169	
t Critical two-tail	1.986	

When comparing the tombstoned components to the sample, the statistical analysis indicated no statistically significant difference. This is made even more apparent when the tombstoned components are compared to just the components that were soldered successfully (Figures 9 & 10).

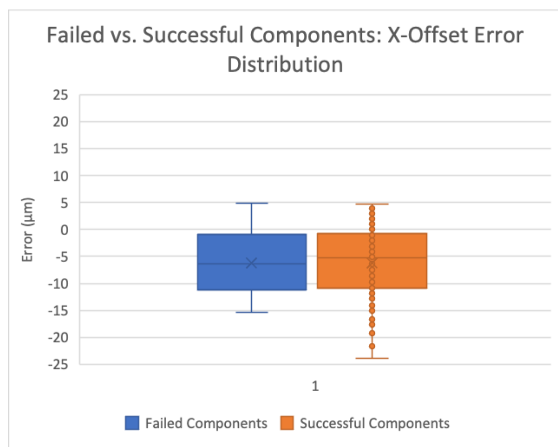


Figure 9: Failed vs. Successful Components X Offset Error

Table 9: X Offset, Successful Components vs. Failed Components, Two Sample t-Test

t-Test: Two-Sample Assuming Unequal Variances		
Successful components vs. failed components (X offset)		
	Variable 1	*Variable 2*
Mean	-6.182	-6.181
Variance	32.826	40.789
Observations	60	180
Hypothesized Mean Difference	0	
df	112	
t Stat	-0.001	
P(T<=t) one-tail	0.499	
t Critical one-tail	1.659	
P(T<=t) two-tail	0.999	
t Critical two-tail	1.981	

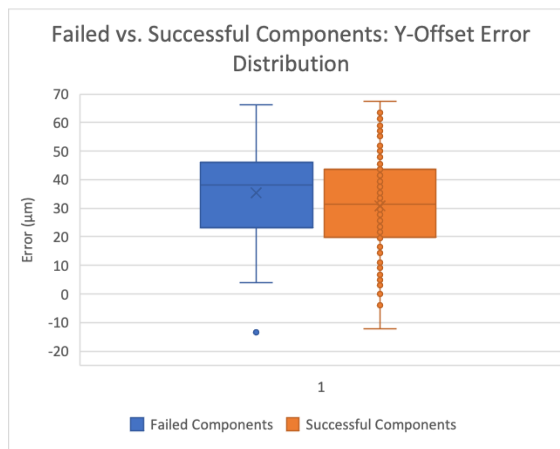


Figure 10: Failed vs. Successful Components Y Offset Error

Table 10: Y Offset, Successful Components vs. Failed Components, Two Sample t-Test

t-Test: Two-Sample Assuming Unequal Variances		
Successful components vs. failed components (Y offset)		
	Variable 1	*Variable 2*
Mean	35.408	30.926
Variance	279.780	292.369
Observations	60	180
Hypothesized Mean Difference	0	
df	103	
t Stat	1.788	
P(T<=t) one-tail	0.038	
t Critical one-tail	1.660	
P(T<=t) two-tail	0.077	
t Critical two-tail	1.983	

The above Tables 9 &10 resulted in a p-value greater than 0.05, meaning there is no statistically significant difference in offset between the components that failed vs. those that didn't. Taking this one final step further, since this analysis was concerned with the magnitude of the offset and not necessarily its direction, a final two sample t-test was run using the absolute value of each offset value.

Table 11: Absolute X Offset, Successful Components vs. Failed Components, Two Sample t-Test

t-Test: Two-Sample Assuming Unequal Variances		
Successful components vs. failed components (Absolute X offset)		
	Variable 1	*Variable 2*
Mean	6.903	6.892
Variance	23.234	31.431
Observations	60	180
Hypothesized Mean Difference	0	
df	116	
t Stat	0.014	
P(T<=t) one-tail	0.495	
t Critical one-tail	1.658	
P(T<=t) two-tail	0.989	
t Critical two-tail	1.981	

Table 12: Absolute Y Offset, Successful Components vs. Failed Components, Two Sample t-Test

t-Test: Two-Sample Assuming Unequal Variances		
Successful components vs. failed components (Absolute Y offset)		
	Variable 1	*Variable 2*
Mean	35.855	31.219
Variance	247.422	274.024
Observations	60	180
Hypothesized Mean Difference	0	
df	106	
t Stat	1.951	
P(T<=t) one-tail	0.027	
t Critical one-tail	1.659	
P(T<=t) two-tail	0.054	
t Critical two-tail	1.983	

Tables 11 & 12 show the results of the t-test and, once again, the p-values of each exceed the level of significance of the test (0.05), indicating no significant difference, even biasing data favorably, and this is consistent with the subsequent boxplot of the data.

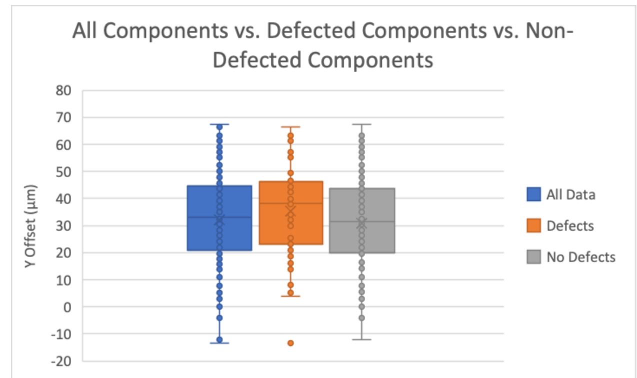


Figure 11: Group 4 Boxplot, All vs. Failed vs. Successful Components

The above boxplot, Figure 11, shows that the components that failed had a smaller distribution of offset than the rest of the sample, but no indication of anything different that would lead to component failure. With the general offsets between good and bad components appearing to offer no trends, the offset of solder paste by its position in the group was graphed to see if any trends would be revealed.

The offset data was further plotted for each board in the X and Y-axis for Group 4. While the graphs shown in Figures 12 & 14 display a random distribution around a linear and level line, Figure 13 & 15 show something far more interesting. Every pairing of solder paste offsets had a difference of about 15-30 µm, resulting in a sine-like wave when shown graphically. Furthermore, this trend only appeared in the Y-axis of the components. This meant that solder paste deposits for a component were consistently positioned slightly farther apart than intended.

This trend, however, was present in both component orientations. This meant that it could not be responsible for the large number of defects observed, as component failure had only occurred in the 90˚ orientation, whereas this factor would have been expected to cause defects in both.

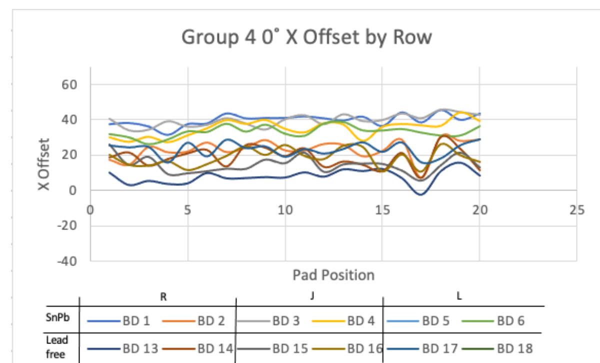


Figure 12: Group 4, 0˚ Orientation, Solder Paste X Offset in the component co-sys by Row

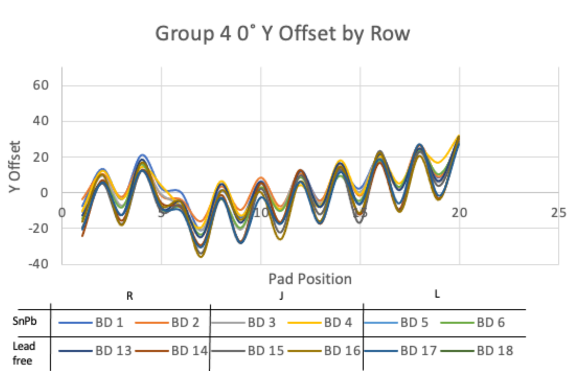


Figure 13: Group 4, 0˚ Orientation, Solder Paste Y Offset in the component co-sys by Row

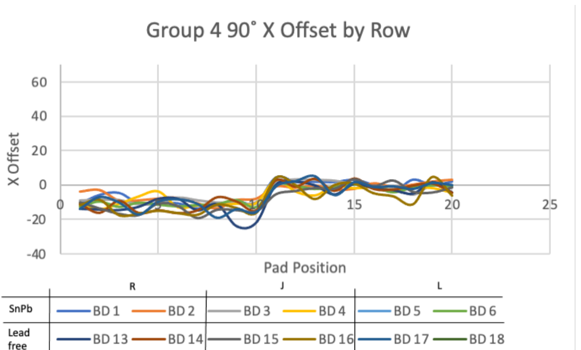


Figure 14: Group 4, 90˚ Orientation, Solder Paste X Offset in the component co-sys by Row

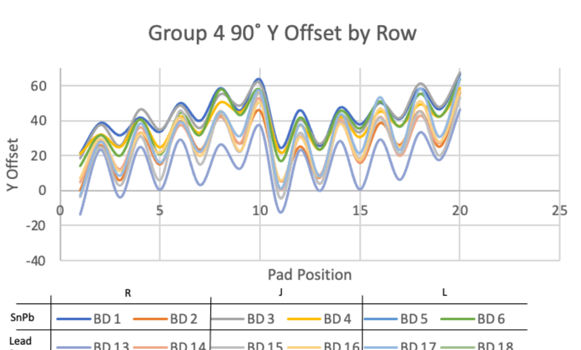


Figure 15: Group 4, 90˚ Orientation, Solder Paste Y Offset in the component co-sys by Row

After finding no evidence that the precision of the solder pastes nor the manner in which the solder is initially deposited onto the PCB was responsible for the defects, the experimental setup and results were once again reexamined. This time, the fact that the defects in the original study had only occurred in the 90˚ orientation was farther examined. Recall that the initial conclusion had speculated that the failure was due to the shape of the solder paste being sensitive to offsets in the Y-axis, but that didn't explain why defects appeared exclusively in one orientation.

Looking again at the direction in which the offset was placed, a question was asked: In what order did each pad of a component reflow in the 90˚ orientation versus the 0˚ orientation?

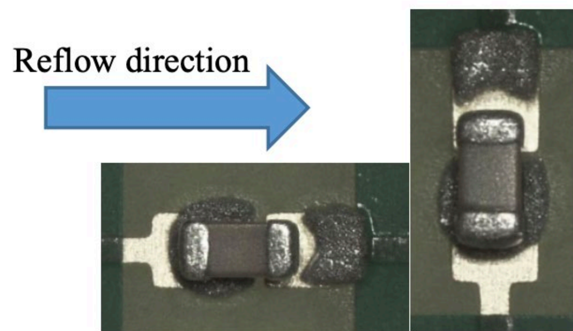


Figure 16: Original 0˚ (left) and 90˚ (right) Component Orientation When Sent Through Reflow Oven

Figure 16 shows the orientation in which the components pass through the reflow oven, where heating initially begins at the right and gradually moves leftward. The new theory proposes that if the heating starts on the right, then the solder paste positioned farther away from the component melts first and has a chance to flow and reach the component before the solder paste on the left melts and pulls the component away. However, the components oriented 90˚ have the solder paste on both sides melt simultaneously, not providing ample time for the farther paste to flow, thus resulting in a tombstone.

To test this theory, two additional boards were printed with conditions that matched the parameters of group 4 – 0% offset in the component's X-axis and 25% offset in the component's Y-axis, however, the only difference was that the PCB would be sent through the reflow oven oriented 90˚ counterclockwise. If the difference in when each pad was heated really was the reason that no defects had occurred in the original 0˚ orientation, then rotating them so that were reflowed in the same way that the 90˚ oriented components had been should yield tombstones. Similarly, now that the 90˚ components were given a 0˚ orientation and the solder paste offset was in the opposite direction, defects should be expected even though this reflow orientation had initially shown none. In other words, the components in the labeled 0˚ area – now adjusted to sit at 90˚ – should see failure rates similar to what was observed in the original study's 90˚ orientation and the components in the labeled 90˚ area – now at 0˚ – should see even more defects.

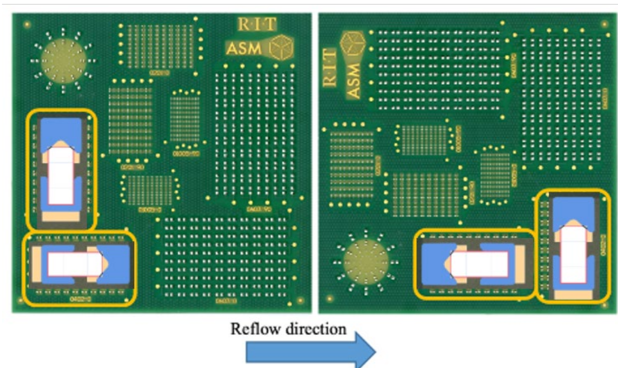


Figure 17: Test PCB Original Reflow Orientation (left) vs. New Reflow Orientation (right)

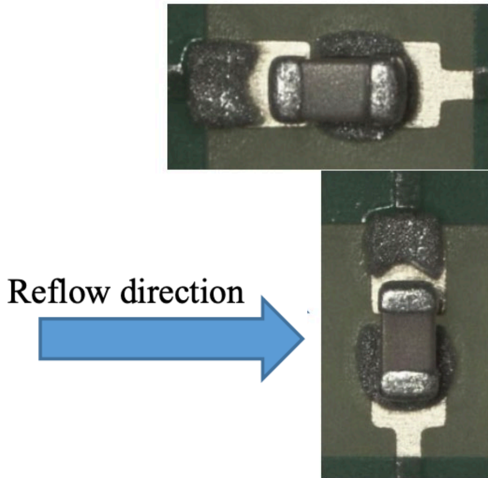


Figure 18: Adjusted 0˚ and 90˚ Component Orientation When Sent Through Reflow Oven

Only one type of solder paste and one component type was used for the new test PCBs, since each was shown to have very little influence on the probability of defects in the initial study. This experiment specifically was only concerned with the occurrence of defects at otherwise equal conditions and not their variable frequency.

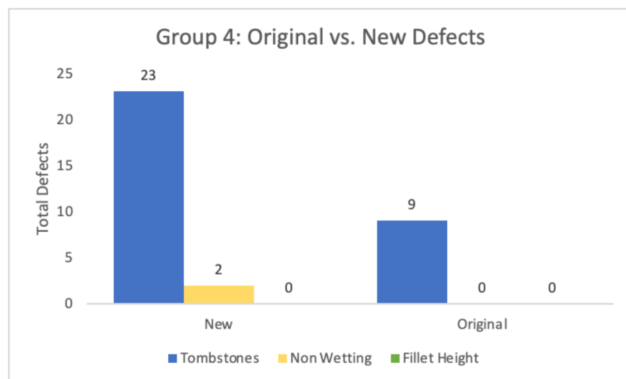


Figure 19: Group 4 Original vs. New Reflow Defect Summary

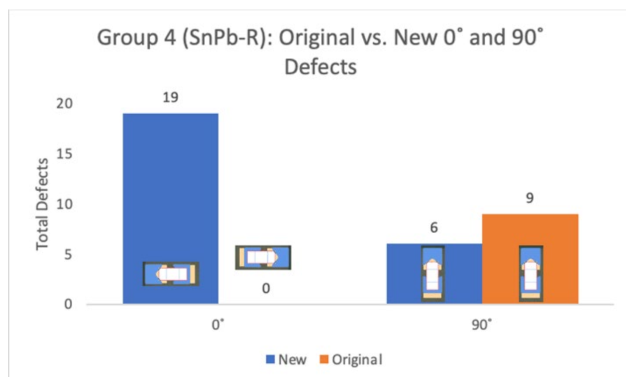


Figure 20: Group 4 Original vs. New Reflow Orientation Defect Summary

Figure 19 shows the occurrence of each type of defect in the original test against the new reflow orientation. Far more defects occurred with the new reflow orientation. To get a better idea of where defects occurred, Figure 20 shows the total defects in each test by the component orientation during the reflow process. Where in the original study, no defects were observed in the 0˚ orientation – even across all three components and solder paste types – in the new test, 19 of the 20 components tombstoned and only 1 of the 20 didn't possess a defect of any kind. Moreover, the components positioned in the 0˚ orientation area of the PCB began displaying tombstones, even though all that was changed was the reflow orientation.

CONCLUSION

The statistical analysis revealed the positional accuracy of the printed solder paste. Though the analysis did show a significant error in positional accuracy, the two-sample t-tests revealed no significant differences in accuracy between the components that tombstoned vs. the ones that did not. This was consistent when both the real and absolute value of the offsets were compared. In other words, there is no evidence that indicates that random positional inaccuracies produced during printing were the cause of the high rates of tombstoning produced when given a 25% offset in the component's Y-axis.

Similarly, though Figures 13 and 15 show a compelling trend in solder paste precision, the difference in position from the nominal value averages out at only about 6%. And regardless of that, this trend in offset was present in all of the components, whether or not they possessed a defect.

Merely changing the orientation of the PCB when sending it through the reflow oven, and thus changing the reflow direction, had a surprisingly strong effects on the results of the process. Originally, the components oriented at 0˚ displayed no tombstones at all. However, when those same components were subjected to reflow with a 90˚ orientation, tombstone defects were observed in that same section of the PCB, even though every other factor had remained the same. Even more intriguing is that when components were reflowed at 0˚, but with solder paste offset directed in the opposite direction almost all of them displayed defects.

This study strongly supports the observation that reflow direction is a major factor in determining whether or not components printed with a bowtie solder paste shape will fail, even if the print offset still technically lies within acceptable standards. It is even more important to note that this effect can be both helpful or harmful, as it led to almost no components failing at the 0˚ orientation in the original study and nearly every component at the same reflow orientation failing in this study.

Printing bowtie deposits can result in one end of a component having a larger degree of contact with the solder paste than the other end. This significantly raises the likelihood of defects, regardless of which way the

offset is biased.

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