Board Level Reliability Testing of RF Packages

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Abstract
Board level reliability testing is becoming a requirement amongst users for acceptance of components and packages. Standard component level JEDEC tests are not sufficient to qualify a supplier, this must be accompanied with board level reliability data to ensure assembly and field reliability. The paper presents a summary of board level reliability test performed on RF packages, the assembly process controls and monitoring, mechanical and environmental reliability tests, understanding of failure modes and lessons learned.

Introduction

Board Level Reliability Test (BLRT) is also known as an interconnect reliability test. This is a method used to evaluate the quality and reliability of solder connections after mounting an IC package to a printed board (PB) for various electronics packages such as IC and area array packages (BGA, CSP, WLCSP, etc.). The reliability of the solder joint during thermal cycling test is a critical issue. The typical thermal cycling condition required for BLRT is from -40°C to +125°C. [1,2] This is to ensure reliable package performance under extreme operating conditions. The current trend for BLRT is to do a combination of environmental and mechanical shock tests to ensure assembly will survive in the field. In most cases, these are user defined tests with specified acceptance criteria that suppliers are required to meet prior to manufacturing release. The paper presents the testing of Wafer Level Chip Scale Package (WLCSP) RF switches through BLRT tests and reviews the process controls, test results, failure modes and lessons learned.

Overview of WLCSP Package and Assembly Process Flow

The WLCSP package assembly includes wafer probe, wafer bump, back grinding, laser mark, wafer saw, singulation and tape and reel of dies. Since the IC is bumped with 200 um bumps and the pitch is 400-500 microns, these packages are not mounted on an interposer or overmolded, as they are directly surface mounted. Fig.1 and Fig.2 show the top and back view of a WLCSP package.

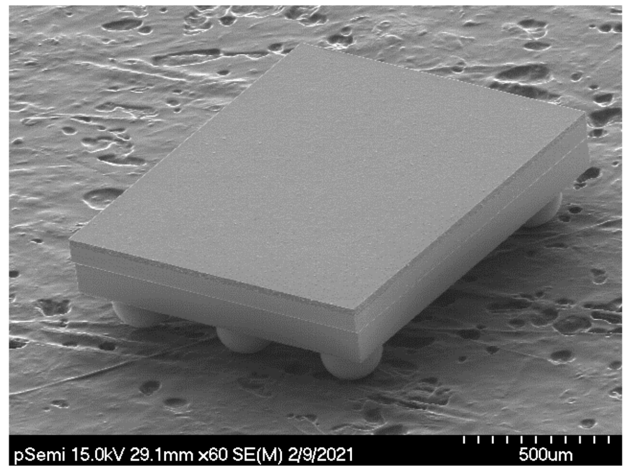

Figure 1. WLCSP Top View

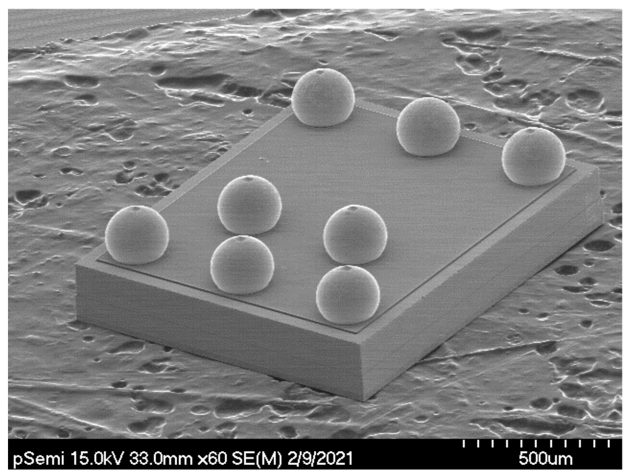

Figure 2. WLCSP Bottom View

The WLCSP typical package dimensions are as shown in Table 1

Table 1. WLCSP Typical Dimensions

Item	Description
Typical Package Dimension	1.16 x 1.36 x 0.39 mm
Bump Diameter	0.208 mm
Bump Height	0.164 mm
Min. Bump Pitch	0.400 mm
# Of pins	6-8 pins

Package attributes were measured for each of the lots that were used in BLRT test as baseline data.

Test-Vehicle PCB substrate

The PCB is a user defined substrate 106mm x 34mm x 0.8 mm thick. It is a 10-layer board. The laminate is low Dk (Dk 3.2 – 3.8 @1 GHz) with minimum Tg of 145 C and minimum Td of 320C. The surface finish on the PCB is OSP. The land pattern is 1:1 ratio for Cu package pads with PCB pads. The trace width /spacing is 150um/125 um. Underfill was not applied post reflow. The flip chip pad diameter was 170um nominal and the NSMD Solder resist opening was 250 um nominal. The copper balance requirement was 40% in the outer two layers and 70% in the internal six layers. Cu foil thickness was 16, 31 and 35 ums. Fig. 3 shows an example of the BLRT test board.

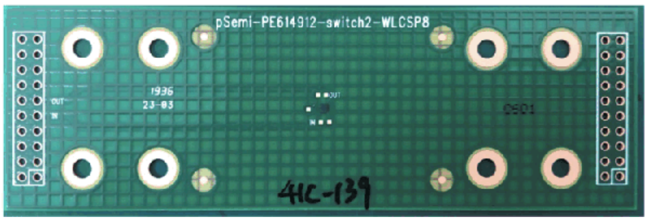

Figure 3. Test-Vehicle Assembly

Die Configuration

The typical die configuration for board level reliability testing is a daisy chain die where alternate pins are shorted to facilitate continuity check. This configuration also allows for in-situ monitoring of the assemblies during the test. Customer protocols for daisy chain die design must be followed to allow for monitoring of various levels of stress on the solder joints. Fig. 4 is an example of bumped die and Fig.5 is an example of a daisy chain die. A PCB schematic is generated to show the connection of the traces from the bump to the connector on the PCB. After initial tests using daisy chain dies, future configurations will be evaluated as product dies which require a different test protocol.

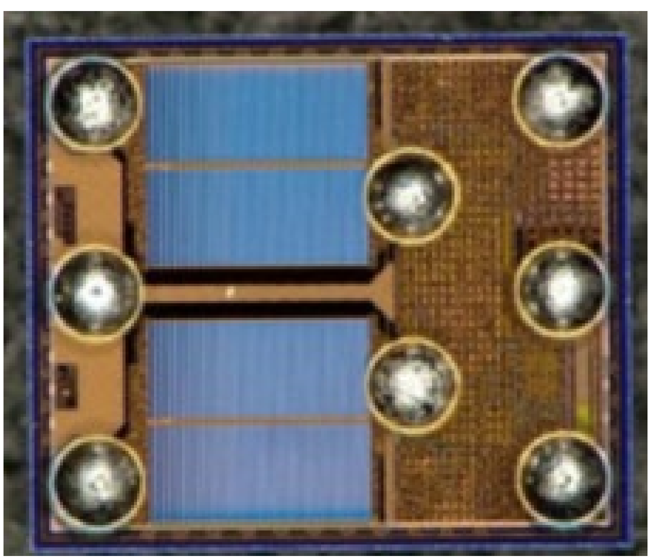

Figure 4. Bumped die

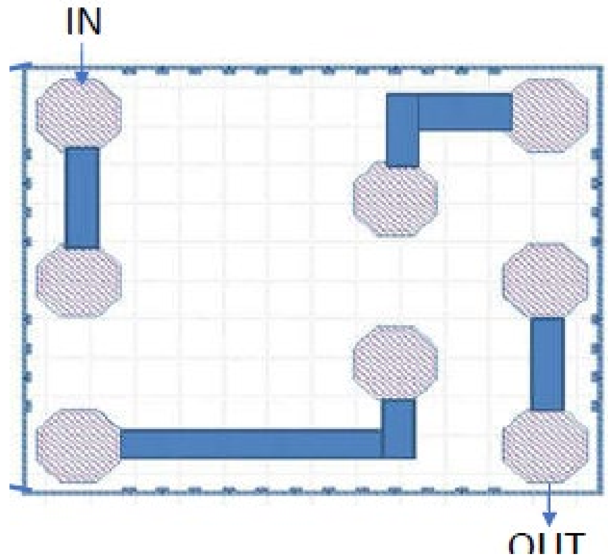

Figure 5. Daisy chain die

Board Assembly

The dies were assembled using surface mount process and lead free reflow. SAC-305 no clean paste was used for package soldering. Stencil openings were 1:1 with substrate pad. Lead free reflow was done at a peak temperature of 248C. The first article analysis was conducted using X-ray and cross -sectioning of the first assemblies to ensure solder joints were intact before the lots were released for assembly. All samples were 100% visually inspected and X-rayed post assembly. No underfill was applied post reflow.

Fig. 6 shows the X-ray post assembly. First article cross-sections were conducted on the assembly to ensure that the interconnect was reliable. Fig. 7 shows the cross-section of the solder joints. Past trial BLRT tests had shown some solderability workmanship issues, so process controls for this assembly were closely monitored for PCB fabrication and assembly.

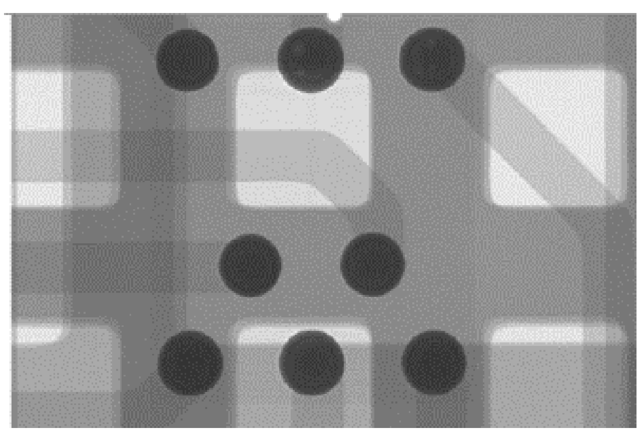

Figure 6. X-Ray of assembly

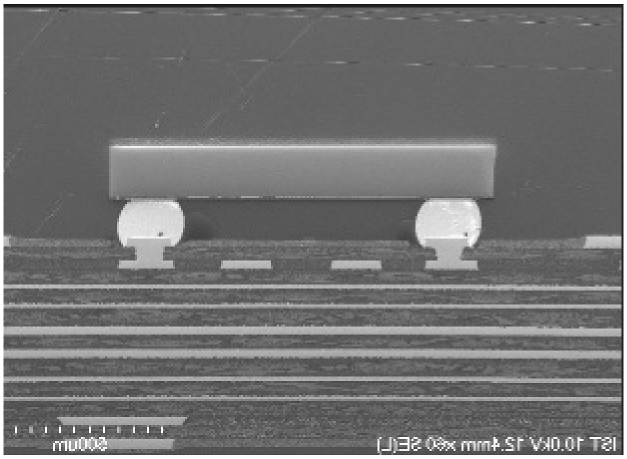

Figure 7. Cross-section of assembly

Assemblies were then subjected to a dry run of test operation to ensure that the PCB and package were functional before conducting lot assembly.

Reliability Testing

The current trend for BLRT test is a combination of environmental and mechanical tests. The following reliability tests were conducted as shown in Table 2.

Table 2. Reliability Tests

Test	Specifications
Thermal Cycling	IPC-9701A [2]
Temp. Humidity Dwell	JESD22A101 [5]
Mechanical Shock	JESD22-B111/IPC-9703[4]
Random Vibration	JESD22B103 [6]
Monotonic Bend	IPC/JEDEC -9702[3]

The BLRT test conditions are as shown in Table 3

Table 3. BLRT Test Conditions

Stress Test	Stress Condition
TC- Thermal cycling	(-40C to +85C) 1,000 cycles
Temperature/Humidity	85C/85%RH – 1000 hours
Random Vibration	5G, 5-500Hz, X/Y/Z- Axis, 30 mins per axis
Mechanical Shock	Shock pulse 5KG, duration 0.25ms, 9 impacts in +Z/-Z
Monotonic Bend	Instron push to fail or stop at 5000uE at 2mm/min speed

The BLRT test also included two bump supplier configurations and two backend process configurations, so the tests were conducted for each configuration as shown in Table 4.

Table 4. BLRT test configuration

Configuration	Process Flow
Bump Supplier A	Backend process flow C
Bump Supplier B	Backend process flow D

The acceptance criteria for the above test are <10% change in resistance post- test except for Monotonic Bend where the acceptance criteria are strain at first package fail is > 4000 uE.

Mechanical shock test set up.

The mechanical test is a critical test and the correct set up is critical for accurate results. The set up for the strain gage measurement is shown in Fig. 8.

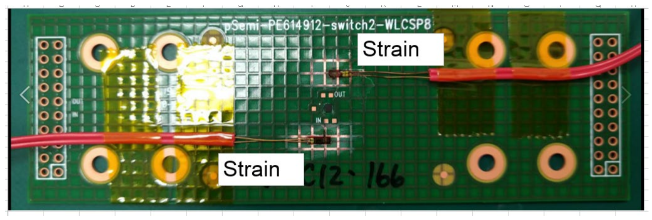

Figure 8. Mechanical Shock Test Set Up

The shock profile is shown in the example below in Fig 9. The shock pulse is 5KG and 0.25 millisecond duration. This test requires at least three samples per lot.

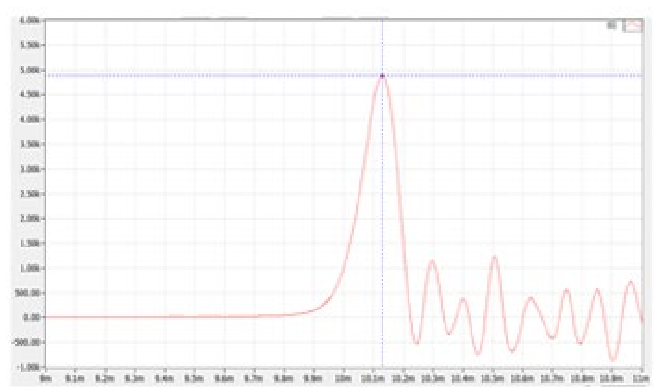

Figure 9. Shock profile for mechanical test.

Per the IPC 9703 test method, for mechanical shock, the +Z and-Z position are shown in Fig. 10 and Fig. 11. In the +Z position, the package is facing up (live bug) and in the -Z position the package is facing down. (Dead bug) position.

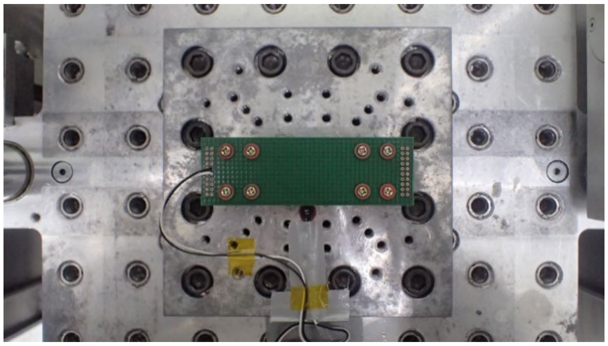

Figure 10. + Z position (Live Bug)

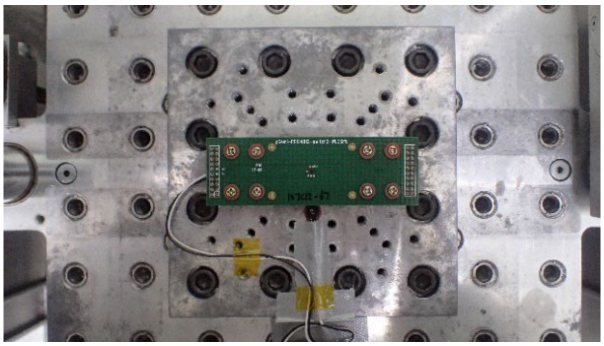

Figure11. -Z position (Dead Bug)

The pre and post resistance test measurements are conducted in-situ and monitored for change in resistance less than 10% as shown in Table 4. This is done for 9 impacts/package of +Z and 9 impacts per package for -Z orientation. All samples met this requirement.

Other Tests

The thermal cycling and temp. humidity tests were performed and passed resistance test measurements. The monotonic bend and random vibration tests were performed per the test conditions and passed resistance measurements. In general, some minor damage was seen on PCB corners and traces due to handling issues during transportation of assemblies to test facility. This was controlled by conducting an audit and improving packaging and providing training for proper handling of assemblies.

BLRT Test Results

The BLRT test was done using daisy chain dies. This version is easier to manage as all the data could be taken in- situ for the duration of the test. Trial runs were conducted to gain an understanding of the failure modes, process controls and test challenges.

A variety of failure modes were seen in the early trial runs due to surface mount workmanship issues. Some of the defects seen were bump cracking, head in pillow, minimal intermetallic formation, voids, solder mask misregistration etc. resulting in five failures in thermal cycling and seven mechanical shock failures. Fig. 12 shows the "Head in Pillow" defect and Fig. 13 shows bump separation due to no IMC formation.

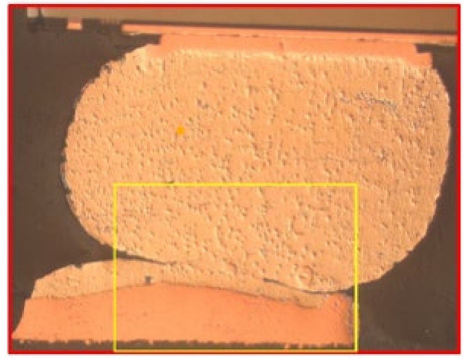

Figure12. "Head in Pillow"

Figure 13. No- IMC formation

The "Head in Pillow" condition was due to an unoptimized reflow profile resulting in early flux evaporation and lack of coalescence between bump and paste solder. The pre heat ramp rate was adjusted to minimize early loss of flux and enable proper coalescence. The "No IMC" issue was due to insufficient coverage of Nickel with Gold surface finish resulting in no IMC formation during assembly. The PCB supplier had to increase time in the plating bath to ensure proper coverage of gold. We learned that optimized PCB processes and SMT process controls were extremely critical to the success of BLRT test. Additionally packaging and handling controls are also essential in maintaining the integrity of the solder joints.

For product test using daisy chain dies, assembly supplier was changed, and first articles were conducted at each step of the assembly process and prior to test set up.

The combination of Bump supplier A and backend process flow C(outsource) and bump supplier B and backend process flow D (in-house) both passed BLRT tests as shown in Table 5 and Table 6.

Table 5. Bump supplier A- Backend Process Flow C

Pass/Fail	Test
Pass 99/99 units	Thermal Cycling
Pass 99/99 units	Temp. Humidity Dwell
Pass 99/99 units	Mechanical Shock
Pass 99/99 units	Random Vibration
Pass 99/99 units	Monotonic Bend

Table 6. Bump supplier B- backend process flow D

Pass/Fail	Test
Pass 99/99 units	Thermal Cycling
Pass 99/99 units	Temp. Humidity Dwell
Pass 99/99 units	Mechanical Shock
Pass 99/99 units	Random Vibration
Pass 99/99 units	Monotonic Bend

Cross-Sectional Analysis

The cross-sectional analysis was conducted on one unit form each passed lot to validate the integrity of the solder joints. Fig.14, Fig.15, Fig.16, Fig.17 and Fig.18 shows the cross-sectional analysis of passed units for mechanical shock, random vibration, monotonic bend, thermal cycling, and temperature humidity. Solder joints met the acceptance criteria per IPC-610. No obvious anomaly was found. Voiding was minimal and less than 30% per IPC-610. Solder joint quality was much improved and much more robust to survive the mechanical and environmental tests.

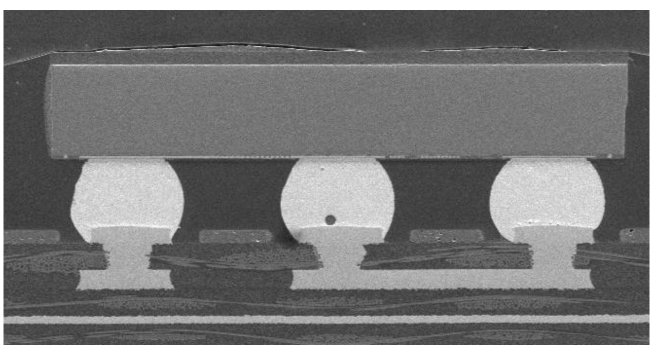

Figure 14. Mechanical shock – passed unit.

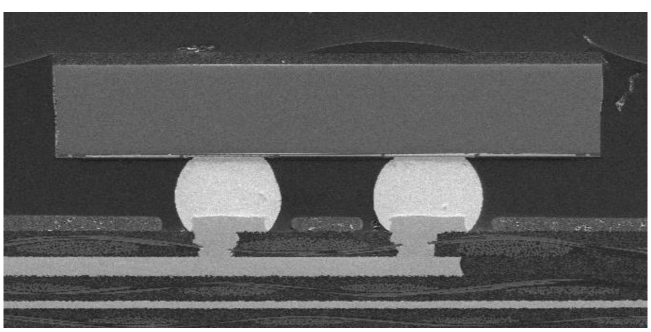

Figure 15. Random Vib- passed unit.

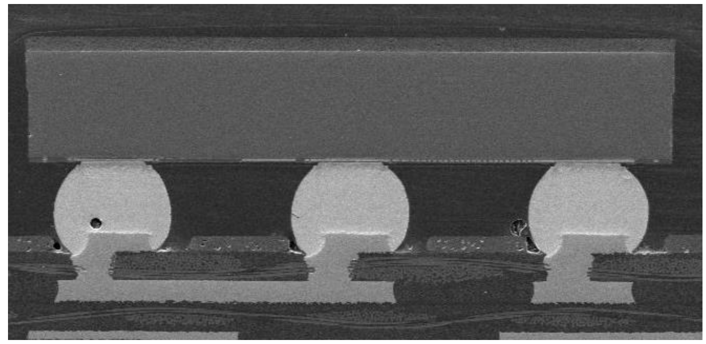

Figure 16. Monotonic Bend

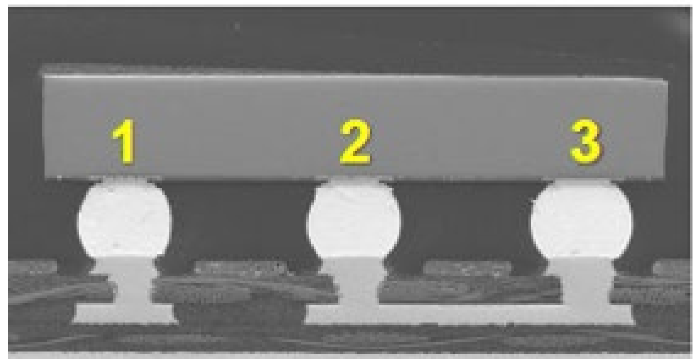

Figure 17. Thermal Cycle

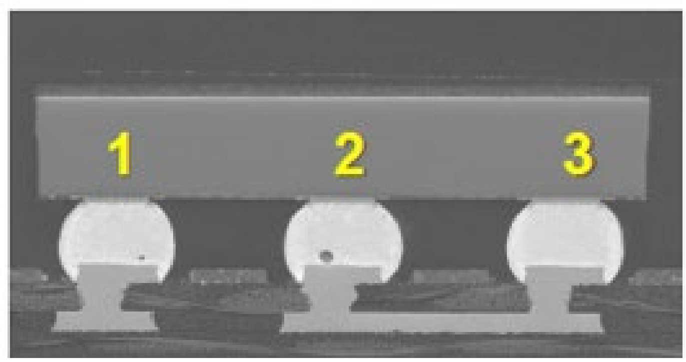

Figure 18. Temp. Humidity test

Lessons Learned

Component, board fabrication and assembly process controls are critical for success of the BLRT test.

It is important to closely monitor PCB fabrication steps and conduct assembly first articles. Document all lot history for inspection, X-Ray analysis and cross-section data before using lots for reliability test. Test facilities with experience in both mechanical and environmental testing should be used. It is preferable to have facilities that conduct all testing in-house, instead of outsourcing as some controls can be lost in that effort and response can be slow. For customer audits, it is preferred to conduct all testing in one facility. The support of an experienced failure analysis lab is essential to understand the various failure modes and identification of root-cause.

Conclusion

Board level reliability tests can be done successfully with proper planning and execution of process, materials, and equipment controls. BLRT is a customized test, so understanding of package geometry, board interactions, material properties and test conditions can provide reliable results. As semiconductor packages diversify and advanced packages increase in complexity, the stresses they experience become more complex. A good understanding of the use environment, customer expectations and accurate testing can provide success in field reliability.

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[4] IPC/JEDEC -9703 -Mechanical shock test Guideline for Solder Joint Reliability.

[5] JEDEC-JESD22A101D.01 – Steady State Temperature Humidity Bias Life Test

[6] JEDEC-JESD22B103B.01- Vibration, Variable Frequency