# Additive Manufactured Electronics for Next Generation Microelectronics

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**ABSTRACT**
As next-generation electronics are developed, several challenges must be addressed as more functions are packed into smaller spaces. These devices will require improved thermal handling due to increased heat generation from active components. Additionally, next-generation technologies, such as 6G, will operate at higher frequencies, posing additional challenges for substrates, which require smoother surfaces. Materials and processes must evolve to meet the RF and conductivity performance requirements.

Additive Manufactured Electronics (AME) has the potential to address the new challenges given the fundamental advantage of the 3rd dimension. Traditional additive implies a layer-by-layer approach which is effective to fabricate 3D shapes, but in addition to the layer-by-layer, it is also feasible to add in a conformal nature over curved and doubly curved surfaces. These provide unique opportunities to fabricate 3D electronics, but the performance of these must be evaluated to demonstrate that the AME approach can compete from an electrically functional perspective. We will examine and contrast some basic devices fabricated with AME and compare to a traditional PCB approach to demonstrate the effectiveness of the approach.

Key words: Additive Manufactured Electronics (AME), Direct write, micro-dispensing, FFF, 3DHI, SiP, Direct digital manufacturing.

**INTRODUCTION**
Next generation microelectronics will be denser and more volumetrically optimized. Stacking of electronic chips for 3D Heterogenous Integration (3DHI) and System in a Package (SiP) are common but is limited due to materials and current processes. The development of advanced materials, particularly those with tunable properties for specific applications, plays a crucial role in overcoming these limitations. Additionally, there is a need for new tools and processes to accommodate the 3D package. Additive Manufactured Electronics (AME) approaches provide a unique opportunity for 3D stacking and printing using a diverse material set for enhanced results.

AME allows for fine features to be patterned onto substrates using a direct printing process, starting directly from a CAD file. These fine features are important when high density is the goal. Several toolheads are used for AME, including micro-dispensing, which can print lines ranging from 20 microns to hundreds of microns in width, enabling the creation of fine interconnects, including in multiple dimensions. The dielectric material serves two purposes, electrical and mechanical. The electrical properties are important from DC to RF, but the RF regime becomes more sensitive to the properties of the dielectric. Mechanically, the dielectric material also provides structural support. The combination of conductive and dielectric materials can create a monolithic composite, potentially eliminating the need for external wiring.

Adding active components to the monolithic composite is similar to adding a defect in a composite material. This can mechanically weaken the structure which imposes additional considerations. Once the active component is mechanically secured, it will be important to maintain electrical connectivity. For small packages such as a QFN (Quad Flat No-Lead) package, the pitch can be tight and for the AME approach, solder is replaced by directly printing to the pads. This can be designed in such a way that the entire structure is still a monolithic composite without air gaps or air bridges that solder bumps impose.

This paper will focus on interconnects fabricated using the AME method. Interconnects are the most vulnerable part of a circuit. Two materials sets will be used to fabricate test devices for studying interconnects. A polymer-based dielectric with silver loaded polymer for the conductor and a borosilicate glass substrate with nano particles in silver paste will be used. Additionally, a test device using standard PCB techniques will be used as a baseline for comparison.

## ADDITIVE MANUFACTURED ELECTRONICS

### Background

The development of Additive Manufacturing (AM), commonly known as 3D printing, began in the 1980s. The first patents and commercial systems, such as stereolithography (SLA) developed in 1986, enabled the layer-by-layer creation of objects from digital models, revolutionizing prototyping and small-scale manufacturing [1]. These early AM technologies, primarily focused on rapid prototyping, involved the deposition of material—usually polymers or resins—to build 3D structures. Selective Laser Sintering (SLS), Fused Deposition Modeling (FDM), and Inkjet-based 3D printing soon followed, broadening the range of materials and applications [2].

In parallel, the 1990s saw the emergence of Direct Write technologies, which allowed for the precise deposition of conductive materials and electronic components directly onto substrates. Techniques such as inkjet printing, aerosol spray, and micro-dispensing enabled the creation of directly written electronic components which eliminated the need for traditional masking processes. A significant driver of this technology was the Mesoscopic Integrated Conformal Electronics (MICE) program launched by DARPA in 1999, which aimed to develop the capability to print electronic components like resistors, capacitors, and antennas directly onto both flat and curved surfaces [3, 4, 5]. This marked the beginning of printed electronics as a distinct area of research.

As 3D printing matured through the 2000s, researchers began to explore ways to combine Additive Manufacturing with Direct Write technologies, leading to the development of 3D Printed Electronics. This integration allowed for the creation of functional, three-dimensional electronic devices, such as circuits, sensors, and antennas, embedded within 3D-printed objects. This fusion of technologies opened new possibilities for manufacturing multi-functional electronic devices in sectors ranging from aerospace to healthcare.

Recognizing the growing need for standardization, the IPC formed a committee to address the specific requirements of Additive Manufactured Electronics (AME). AME represents the convergence of 3D printing and printed electronics and is poised for significant growth, with projections indicating a rapid expansion in the coming years [6]. By combining advances in both 3D printing and Direct Write technologies, the field of Additive Manufactured Electronics is transforming how complex electronic devices are designed and manufactured, offering new capabilities for producing lightweight, integrated, and customizable systems.

### Direct Digital Manufacturing

The work presented in this paper uses a combination of several processes in a single tool. Direct Digital Manufacturing (DDM) offers many advantages as a digital process, with one of the main benefits being the elimination of the need for tooling. Traditional manufacturing processes often require expensive tooling and molds, which can take time to produce and modify. DDM skips this, making it easier to rapidly prototype and produce. The DDM system used is from nScrypt and this system has multiple tools with auto tool changing. The tool heads are 3D printing and more specifically using Fused Filament Fabrication (FFF), milling, smoothing, micro-dispensing, pick and place, vision and heating control on a heated plate. DDM will start with a CAD file and in the case of electronics, the CAD file will have details on print patterns and the number of layers and the material type. Material type is set by the tool head chosen. Using FFF as a dielectric and structural material requires a single tool head. For micro-dispensing, there are typically more than one type of material, each having its own tool head. Milling and smoothing can be done with the same tool head, a high-speed mill. The pick-and-place allows for a more complete process for fabricating circuits. The CAD file will have commands for each tool head and process. Using AME and DDM to fabricate circuits requires a specific set of design to manufacturing rules which are different than traditional PCB processes.

### Thermoplastic Materials and Process

The fabrication of the test devices utilizes several methods of manufacturing. Fused Filament Fabrication (FFF) is used to create substrates made of ThermaX™ PEEK 3D Printing Filament from 3DXTech. FFF is an additive manufacturing technique where melted thermoplastic material is extruded through a hot nozzle. FFF is a useful technology due to its fast production speeds, high geometric accuracy, and low material cost.

**Table 1.** Mechanical and Thermal Properties of PEEK [7]

| Property | Value | Unit |
|---|---|---|
| Density | 1.30 | $g/cm^3$ |
| Tensile Strength | 100 | MPa |
| Tensile Modulus | 3720 | MPa |
| Glass Transition Temperature | 143 | °C |
| Deflection Temperature at 0.45MPa | 140 | °C |

Subtractive manufacturing processes are used in conjunction with additive manufacturing to produce the test devices. Specifically, milling is used to machine the surface of the FFF substrates, resulting in smooth and flat top surfaces. In this process, an end mill bit is spun at a calculated RPM to cut away a specified amount of material from the top surface of the workpiece. These components are mounted in the substrates using a pick-and-place operation, where a small vacuum nozzle is used to pick up components and move them to their respective placement locations. The process is enhanced with vision. By using a high-quality camera equipped with a telecentric lens, the picking and placing locations can be identified easily. The components used in the test devices are TopLine QFN16T.5-T-DED1.7 QFN Daisy Chain. The test component is 3 mm x 3 mm with a 500 µm

pitch. This chip contains shorted pairs of pads, allowing for the quality of the interconnects to be evaluated using resistance and continuity. Each resistance measurement measures a pair of interconnects.

Micro-dispensing is the final manufacturing process used to create the test devices. MicroMax™ CB028 and EpoTek® H20E are the pastes used in this process. MicroMax™ CB028 is a thixotropic, silver-loaded conductive paste used for fabrication of conductive interconnects, traces, and pads. EpoTek® H20E is a conductive epoxy used to adhere the pads of the daisy chain chip to the substrate and the conductive traces. These pastes are extruded through a nozzle and dispensed on to a surface. Extrusion is controlled through the pressurization of the paste and the positioning of a valve.

The resistivity of CB028 is about $4.06\times10^{-7}$ Ω·m [8] when cured at 120 °C.

**Table 2.** Properties of MicroMax™ CB028 [9]

| Property | Value | Unit |
|---|---|---|
| Viscosity | 150-300 | P |
| Surface resistivity | $\leq3\times10^{-7}$ | Ω·m |
| Curing Temperature | 160 | °C |
| Curing Time | 60 | min |

**Fabricated Devices**

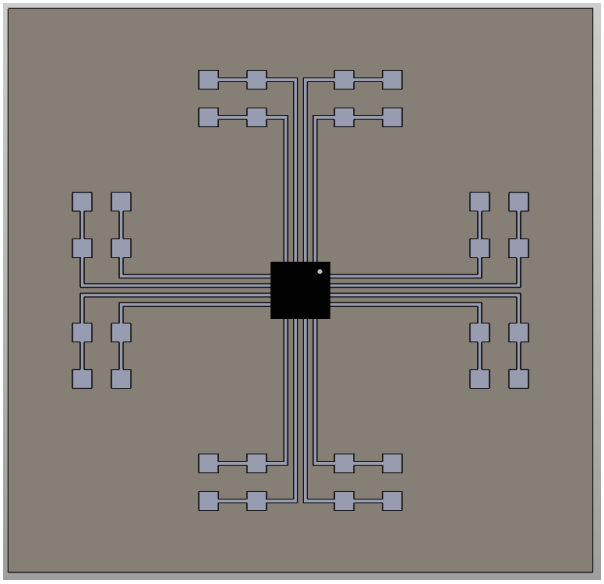

**Figure 1.** CAD of theoretical QFN interconnect design

The test devices were designed in such a way that all of the pads of the QFN were face-down on the PEEK substrate. The resistance of the interconnects is measured reliably and accurately using the four-point probe technique. To do this, two conductive pads for probing are printed per interconnect.

The substrates for the test devices are made of PEEK. 3DXTech ThermaX™ PEEK is extruded out of a high temperature 400 µm ID nozzle onto a heated aluminum bed at 5 mm/s. After the substrate is printed, 50 µm is removed from the surface of the PEEK substrate to ensure a low surface roughness. This is done using a 0.020" carbide mill bit at 20,000 rpm and 5 mm/s. Next the interconnects, traces, and pads are printed with MicroMax™ CB028 on the top surface. The conductive paste is extruded out of a 100 µm ID nozzle at 7 mm/s. The paste is pressurized to 7 psi, and the distance between the open and close position of the valve is 70 µm. Dots of EpoTek® H20E is then dispensed on the interconnects where the pads of the QFN will lie. Before the conductive epoxy dries, a downward facing camera is used to identify the location to pick the QFN up and the location to place the QFN down. This process becomes increasingly important as component packages and pad pitches become smaller. After placing the QFN, the test device is removed from the heated bed and placed in a 120 °C convection oven for 15 minutes to cure the conductive epoxy and silver traces.

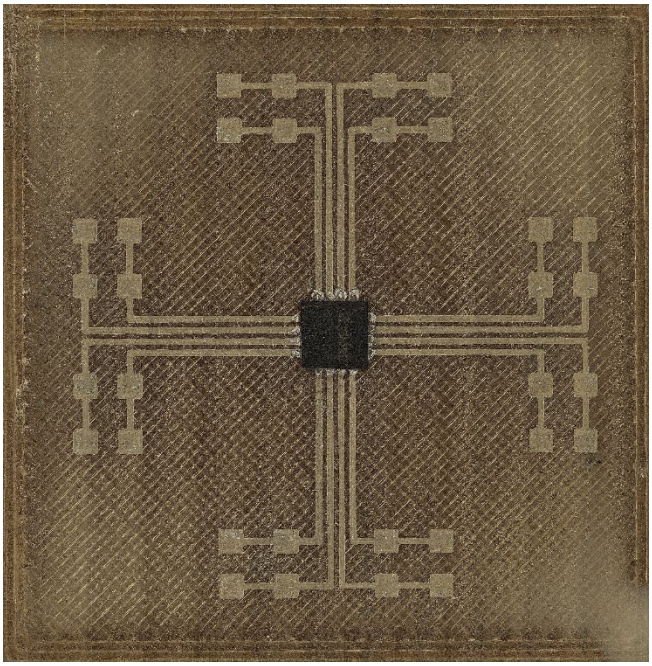

**Figure 2.** Printed QFN test device on PEEK substrate

**Glass Substrate with Nano-paste Materials and Process**

The fabrication of these test devices involves several advanced manufacturing techniques, focusing on the 3D printing of small circuits on glass using silver as the conductive material, without the need for traditional filament. This method deviates from the more common Fused Filament Fabrication (FFF), where melted thermoplastic is extruded to create structures. Instead, a direct-write technique is employed, which is ideal for laying down conductive traces directly onto the glass substrate.

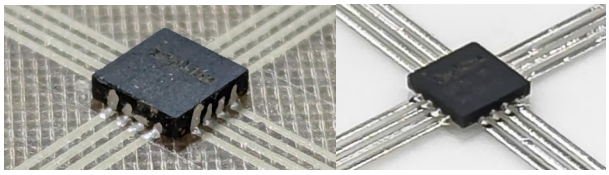

**Figure 3**. Photo of interconnects on PEEK and glass

Silver is the primary conductive material used in this process, chosen for its excellent electrical conductivity and compatibility with glass. The silver is applied using a micro-dispensing process, which allows for precise deposition of silver paste in a controlled manner. This method involves extruding the silver paste through a nozzle, where the pressure and valve positioning regulate the amount of material dispensed. The silver paste is composed of nano silver particles, typically 35-50 nm in diameter. The paste exhibits an electrical resistivity of $4.20\times10^{-8}$ Ω·m, making it highly suitable for electronic applications that require efficient signal transmission.

Once the silver traces have been deposited, a standard QFN chip is placed onto the glass substrate. The chip placement is carried out through a pick-and-place process, which uses a vacuum nozzle to pick up the QFN chip and position it onto the substrate with precision. The accuracy of this process is crucial, as the QFN chip must be perfectly aligned with the pre-deposited silver traces to ensure optimal electrical connections. After the micro-dispensing of the silver paste and the placement of the QFN chip, the next crucial step is curing. The silver traces need to solidify and bond firmly to the glass substrate to create a stable and conductive path between the chip and the external circuit. The heating process involves sintering the nano silver at 250 °C for 40 minutes, which allows the silver particles to fuse and form a continuous conductive layer. This process significantly reduces the resistivity of the material, ensuring that the electrical connections are robust and capable of handling the required current.

Glass, as a substrate material, offers several advantages in this application. It is chemically inert, offers excellent dimensional stability, and has a smooth surface ideal for precision manufacturing. For this particular test device, a 200 µm glass substrate was used. To hold the substrate in place during the manufacturing process, a vacuum bed was used, ensuring that the glass remained stable and flat while the conductive nano silver paste was dispensed. The use of glass also provides transparency, which can be advantageous in certain sensor or optical applications, and its non-conductive nature makes it an excellent insulator for the circuits.

**Table 3.** Mechanical and Thermal Properties of Borosilicate Glass [10]

| Property | Value | Unit |
|---|---|---|
| Density | 2.51 | $g/cm^3$ |
| Tensile Strength | 63.5 | MPa |
| Shear Modulus | 34,000 | MPa |
| Glass Transition Temperature | 557 | °C |
| Softening Point | 550 | °C |

The final product is a highly precise, miniaturized circuit with strong electrical performance, all created without the need for traditional 3D printing filaments or plastic materials. By leveraging advanced micro-dispensing techniques, nano silver conductive pastes, and high-precision alignment tools, this fabrication method offers a streamlined process for developing circuits on non-traditional substrates like glass. This makes it particularly suitable for applications requiring high-performance, small-scale electronics where heat management, durability, and material properties are critical factors.

## RESULTS

The resistances of the PEEK-printed interconnects, fabricated with MicroMax™ CB028 silver-loaded conductive paste, ranged from 2 Ω to 9 Ω, depending on the trace width and thickness. These values are typical for polymer-based conductive materials, where the conductivity is influenced by the silver-loading percentage and the quality of the micro-dispensing process.

In contrast, the interconnects fabricated on the glass substrate using nano silver paste exhibited significantly lower resistance, with measured values ranging from 1 Ω to 4 Ω. This improvement in conductivity can be attributed to the higher silver content (82 %) in the nano silver paste that is sintered and the enhanced deposition precision on the glass surface. The sintering process at 250 °C for 40 minutes further increased conductivity by forming continuous conductive paths between the silver nanoparticles, resulting in superior electrical performance.

In summary, while traditional PCB technologies offer lower resistance and superior conductivity, the AME-fabricated interconnects on glass, particularly those using nano silver paste, approach competitive conductivity levels and offer significant benefits in terms of design flexibility, especially for next-generation electronics requiring complex, multi-dimensional architectures.

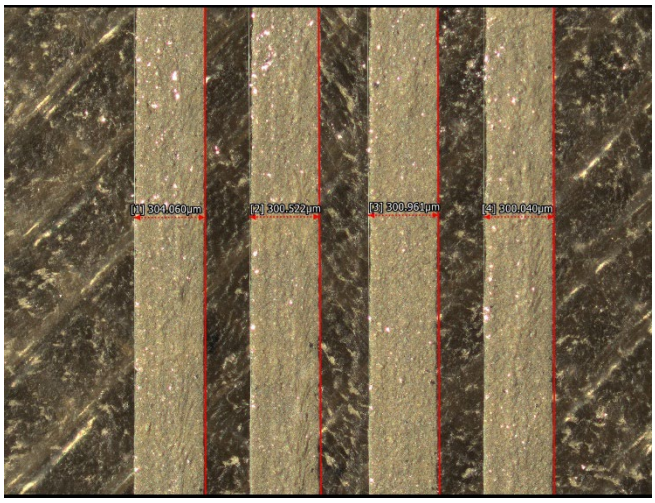


**Figure 4.** MicroMax™ CB028 interconnect line widths

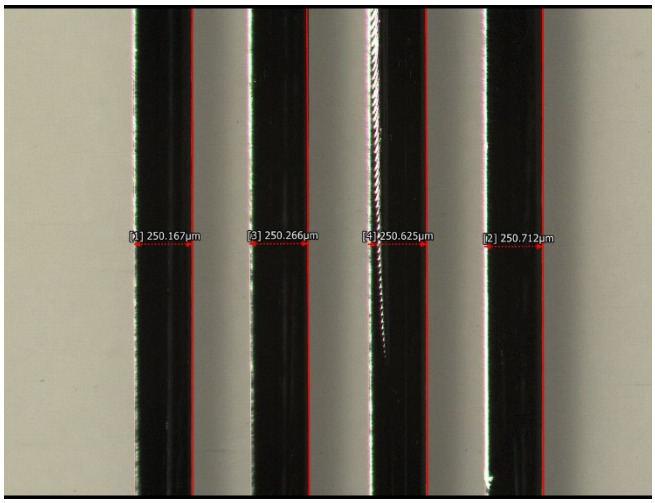


**Figure 5.** Nano-silver interconnect line widths

**Table 4.** Resistance Measurements (Ω)

| Interconnect Pair | CB028 | Nano-paste |
|---|---|---|
| 1 | 5.787 | 1.956 |
| 2 | 7.333 | 1.180 |
| 3 | 4.166 | 4.300 |
| 4 | 5.233 | 2.070 |
| 5 | 7.200 | 2.406 |
| 6 | 8.966 | 3.113 |
| 7 | 3.166 | 1.520 |
| 8 | 2.633 | 1.923 |
| Average | 5.560 | 2.308 |
| Theoretical (trace only) | 2.800 | 0.289 |

The theoretical resistance values are calculated from the data sheet resistivities and dimensions of the conductive traces only. The theoretical resistance values are lower than the measured resistances due to static cross-sectional area and datasheet resistivity throughout the trace. The silver nano-paste shows a 2.4 times improvement in conductivity over CB028. This improvement could grow greater with optimized printing and curing processes.

## CONCLUSION

The study successfully demonstrated the fabrication and evaluation of test devices using Additive Manufactured Electronics (AME) with different materials and manufacturing techniques. Two material sets were explored: a polymer-based dielectric with silver-loaded polymer conductors, and a glass substrate with nano silver particles.

The resistance values varied depending on the material and process used, with the silver nanoparticle paste showing better conductivity compared to the polymer-based conductive material. This confirms that the choice of materials, particularly the percentage of silver content in the conductive paste, plays a critical role in the performance of AME-fabricated circuits. The use of glass as a substrate was advantageous, offering a smooth surface and excellent dimensional stability, which contributed to the precision of the micro-dispensed silver traces. Additionally, the direct-write process on glass produced robust electrical connections, with the sintering process further reducing resistivity.

Overall, the AME approach proved effective in producing high-performance, miniaturized circuits on both polymer and glass substrates. This confirms that AME has the potential to meet the demands of next-generation electronics, where size, performance, and flexibility are crucial. Future work could explore optimizing materials with higher conductivity and refining processes to further enhance the performance of these devices in advanced applications.

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