2nd Generation of indium TIM

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ABSTRACT

Advanced high-power electronic chips can generate substantial heat during operation. Thermal interface materials (TIM) dissipate the generated heat from the die to the lid and facilitate the cooling of the device. Gaps and voids along the joint (die/TIM/lid) cause local discontinuity in the thermal path, decrease thermal conductivity, and reduce TIM effectiveness in thermal management. Indium has been widely used as an excellent TIM material in LGA and PGA packaging. However, as the industry moves towards BGA packaging, utilizing indium as a TIM layer has been challenging. So far, attempts to use indium in BGA packaging have failed due to excessive void formation during inevitable multiple reflow process steps in BGA packaging. In this research, a new generation of indium TIM is introduced. This class of indium TIM has a protective layer to suppress surface oxidation. Therefore, a fluxless reflow process without the assistance of a reduction atmosphere is possible. Study shows the main advantage of this product is significant void reduction, able to reach >95% of the joint coverage, even after multiple high temperature reflow processes. Intermetallic compounds (IMC) formation at the interface of TIM-substrate is also examined and discussed in this work.

Key words: Indium, BGA packaging, TIM, void, voiding

INTRODUCTION

The current trend in the hardware and electronics industry is to make faster devices with higher computational powers, which, in turn, means using electronic chips with higher power densities [1]. To accommodate this market demand, semiconductor manufacturers face new challenges. Larger die sizes are required for the new generation of electronic chips, making thermal management complicated.

Using a highly thermal conductive material at the interface to connect the die and integrated heat spreader (IHS) (commonly referred to as "lid") is the customary practice in electronic packaging. Solder Thermal Interface Materials (STIMs) have been widely used in high-power processors for over two decades. Among them, pure indium is a popular choice for CPUs due to its high thermal conductivity, relatively low melting point, and its unique mechanical properties. Compared to other metals, indium has low tensile strength, low Young's modulus and relatively high fatigue life (gum-like material), which makes it an excellent candidate for TIM, able to absorb stress caused by CTE mismatch of the device components. In 2003, Intel invented thermal Interface Material made of indium [2] and used it in high-power devices. Deppisch et al. later illustrated the application of indium as TIM in CPUs in detail [3]. Since then, indium has been successfully used in Lidded Grid Array (LGA) and Pin Grid Array (PGA) packaging. However, for Ball Grid Array (BGA) packaging, which needs multiple high temperature reflow steps after lid attachment and indium reflow, attempts to use indium as TIM1 have failed. After the initial TIM1 attachment, subsequent reflow processes, such as ball attachment, board mounting, potential rework, etc., are required in BGA packaging. Hence, indium TIM must undergo multiple reflow steps. The peak reflow temperature for these process steps is 240°C- 260°C, considerably higher than the indium melting temperature (157°C). Figure 1 shows a simplified process step demonstration for LGA, PGA, and BGA packaging. It is shown that while indium reflow is the last reflow step for LGA and PGA packaging, in the case of BGA packaging, there are additional reflow steps, all conducted at temperatures above 240 °C. Indium TIM will be remelted during each of these reflow process steps.

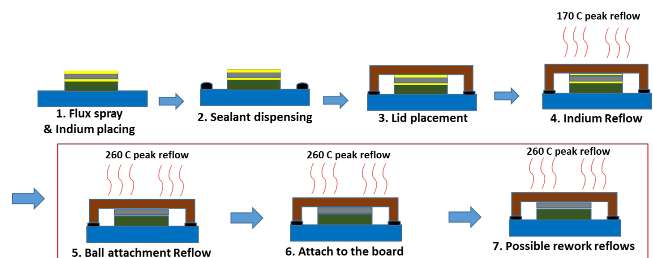

Figure 1. a) Simplified process steps for LGA and PGA packaging, b) additional process steps for BGA packaging

The current attempt to use indium in BGA packaging has failed because excessive voids will form during subsequent high temperature reflow steps. Voids are generated for several reasons. Four major types of voids are shown in Figure 2, and their potential source is listed in Table 1. As shown, a critical group of voids is potentially caused by entrapped residues of chemical flux used to remove indium oxides prior to indium reflow. Chemical fluxes are designed to activate at temperatures below the indium melting point (156.7 C). However, their organic components may be volatile at higher temperatures. It is, in particular, a problem for BGA packaging because any entrapped flux residues after indium reflow can produce gaseous voids during subsequent high temperature (up to 260C) reflow steps. These voids may

expand to larger voids and increase thermal resistance, making the application of indium as TIM ineffective.

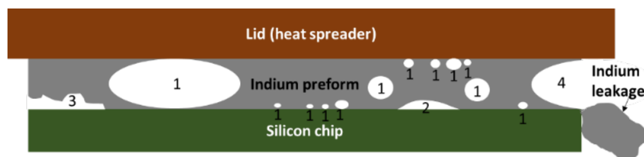

Figure 2. Simplified demonstration of voids at Lid/TIM/Die stack

Table 1. Potential source of voids at Lid/TIM/Die stack

Numbers in the pictures	Types of voids	Possible causes
1	Gas / flux entrapped void	Entrapped flux residue expansion as form of gas during the reflow
2	Dewetting void	Metallization quality / Metallization exhaustion because of reaction
3	Delamination	Stress / warpage / poor interface adhesion / micro alloying
4	"Starving void"	Leakage / Bleeding

The research and Development team at Ningbo SJ Electronics Ltd. has developed a new generation of indium thermal interface material (named" indium Gen II") with a special surface treatment to protect the indium surface from oxidation, so no liquid chemical flux is required to remove the oxides during the indium reflow. In this paper, the performance of this product is studied. Void formation after multiple high temperature reflow for these treated indium TIMs is examined. Also, the result is compared with the case of conventional indium preform and chemical flux when it undergoes similar reflow steps. Intermetallic formation at the interface of indium and substrate is also studied.

MATERIALS AND METHODS

Tests are designed to simulate BGA reflow steps. Test coupons are copper substrates with a Ni/Au plating finish, similar to the "lid" in FCBGA packaging (Figure 3). A polymer-based sealant, similar to lid attachment sealant, is applied. TIM size is relatively large (35 * 20 mm^2), to evaluate its performance for advanced high power density packaging with a larger die size. Table 2 shows the details of the test vehicle and indium TIM, and Table 3 summarizes the DOE to conduct this study. For reference tests, untreated indium preforms, and industrial indium flux is used. As mentioned, using a liquid flux to activate indium Gen II TIM is not required.

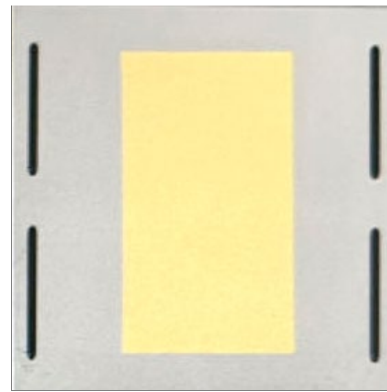

Figure 3. Test coupon for void evaluation

Table 2. Test samples and experiment preparation

Test coupon	**Material:** Copper **Surface finish:** Ni (3-5 µm)/Au (0.4-0.6 µm) **Dimension:** 47 mm * 47 mm* 1mm
Indium Gen II TIM	**Material:** Indium with a protective layer **Dimension:** 35 mm * 20 mm **Thickness:** 230 µm
Reference TIM	**Material:** Indium without the protective layer, plus chemical flux **Dimension:** 35 mm * 20 mm **Thickness:** 230 µm

Table 3. DOE table for void evaluation

LEG	TIM	No. of samples	Indium reflow	BM reflow, 3 times
Leg 1	Untreated indium + flux	16	170°C Peak (W/O Vacuum)	260°C Peak (W/O Vacuum)
Leg 2	Indium Gen II (with a protective layer), No flux	16	170°C Peak (W/O Vacuum)	260°C Peak (W/O Vacuum)

The thermal history of samples is summarized in Table 4. After placement on indium Gen II TIM between two Cu/NiAu substrates, a sealant is used to bond two Cu/NiAu substrates and maintain a predetermined uniform distance between the two substrates. This is similar to the lid attachment step in FCBGA packaging. After lid attachment, indium reflow is conducted at a peak temperature of 170 °C. Then, each sample undergoes high temperature reflow (peak temperature 260 °C) three times, similar to ball attachment/ board mounting process steps.

Table 4. Thermal history of samples

Lid Attachment	**Temperature:** 130 °C **Duration:** 4 minutes
Indium Reflow	**Peak Temperature:** 170 °C **Time above liquidus:** 180 seconds **Atmosphere:** Nitrogen, w/o vacuum
Ball attachment/ board mounting reflow (repeated up to three times)	**Peak Temperature:** 260 °C **Time above liquidus:** 360 seconds **Atmosphere:** Nitrogen, w/o vacuum

After each reflow step, voids are evaluated. Confocal Scanning Acoustic Microscopy (CSAM) is a standard non-destructive test method to detect voids in the electronic industry. In this study, after each reflow step, a CSAM photo of the joint is taken. The void ratio for each sample is calculated based on the CSAM image of the joint. Also, a sample after each reflow is selected for additional cross-section analysis. The sample is cut and polished, and the In/AuNiCu interface is examined using SEM/EDS.

RESULTS AND DISCUSSION

Void formation and propagation

Figure 4 demonstrates the CSAM photo of selected samples after each reflow step. The graph in Figure 5 shows the average void fraction after each reflow step.

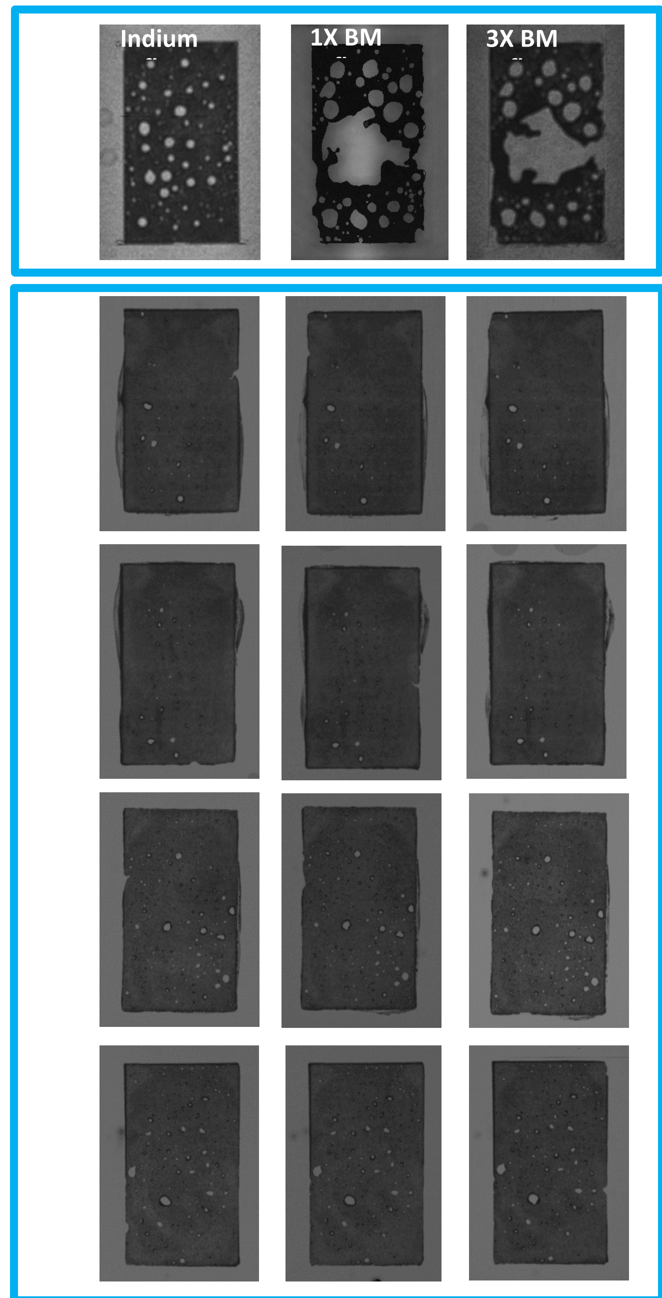

Figure 4. SCAM images of a) Leg 1, untreated indium + flux, b) Leg 2, indium Gen II; after indium reflow, one time of BM reflow, and three times of BM reflow, respectively.

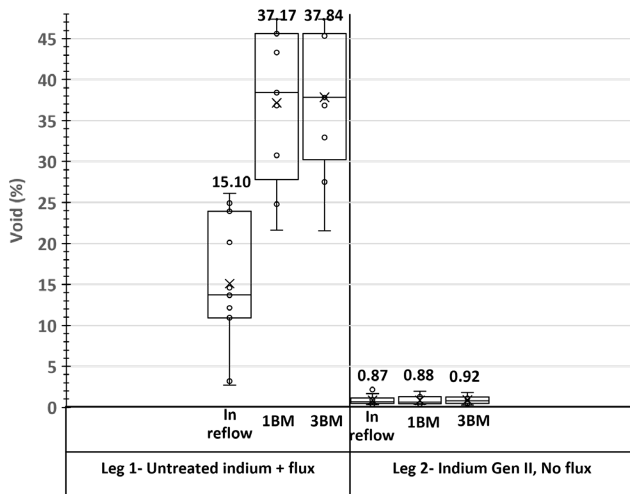

Figure 5. Void percentage after indium reflow, one time of BM reflow, and three times of BM reflow for industry benchmark indium + chemical flux, and indium Gen II without flux

Using a chemical flux to remove oxides and provide a fresh indium surface to wet die/lid substrates may be sufficient for LGA/PGA packaging and small to medium die size. However, as observed in Figures 4 and 5, there is a significant increase in voids after high-temperature BM reflows, and this method is not suitable for BGA packaging. Indium Gen II TIM (with a protective layer) significantly improves void reduction when no liquid flux is used. Even after multiple high temperature reflow processes, there are minimal voids. Although there is no direct method to observe void formation and propagation during reflow, the mechanism of void formation can be predicted and explained. Liquid flux, activated at an approximate temperature of 140 °C- 150 °C, leaves organic residues at the interface after the indium reflow process. These residues are trapped after indium solidification is completed. As demonstrated in Figure 4, they appear in the form of voids after the initial indium reflow step. Some flux residue components may be volatile at temperatures below 260 °C. Decomposition of flux residue during BM reflow steps (peak temperature of 260 °C) leads to the formation of the gaseous phase and further expansion of voids (Figure 6). A cross-section image of the samples after indium reflow and BM reflow supports this explanation of void formation and expansion (Figure 7).

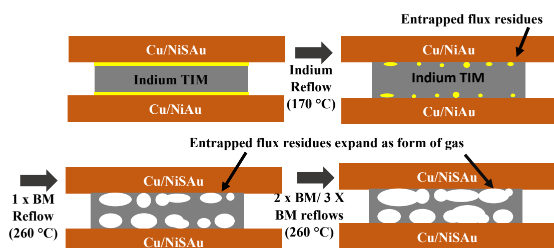

Figure 6. Schematic of void formation at TIM-Cu/NiAu interface during multiple reflow processes

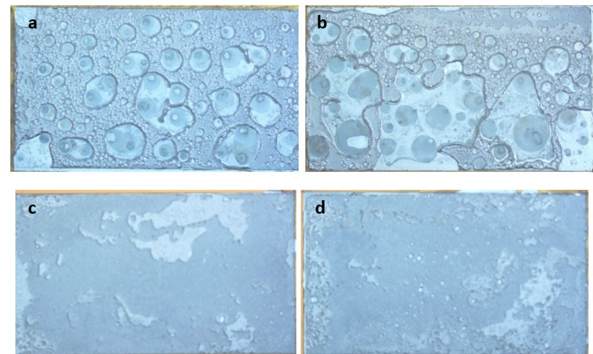

Figure 7. Cross section images of TIM for a) indium + chemical flux after indium reflow (170° C), b) indium + chemical flux after 3 times of BM reflow (260° C), c) indium Gen II w/o flux after indium reflow (170° C), indium Gen II w/o flux after 3 times of BM reflow (260° C)

Indium TIM- Cu/NiAu interface analysis

Figure 8 shows SEM images of In-Cu/NiAu interfaces after the initial indium reflow step and subsequent high-temperature reflow steps. As demonstrated, a thin layer of intermetallic compound (IMC) is formed during initial indium reflow. Ni layer is still mainly intact (approximately 3-5 µm). After the first BM reflow, a continuous layer of IMC is formed. The thickness of this layer is approximately 4-5 micrometers. Additional BM reflows lead to the formation of a thicker IMC layer. In this study, the IMC thickness after three times of reflow is approximately 15-20 micrometers at different areas. An IMC layer is advantageous to maintain the bond between the TIM and substrates. However, since the IMC has different mechanical properties than the solder TIM (generally harder), if this layer is too thick, it can be a source of crack propagation and cause reliability issues over the operation duration of the device. Therefore, optimizing the reflow profile is essential to avoid the IMC layer's excessive growth. Another critical factor to consider is the quality and thickness of Ni and Au layers. If the Au layer is too thin, and Ni is exposed to the atmosphere at a high temperature before indium wets the substrate, voids will form. During high-temperature reflows, the Au layer is expected to be fully consumed. If the Ni layer is too thin, or subsequent BM reflows processes are not optimal (for example, peak temperature is too high, or time above liquidus is too long), and all the Ni layer is consumed, the copper layer will be exposed. In this case, solder TIM will further react with Cu and form a very thick IMC layer as shown in Figure 8.

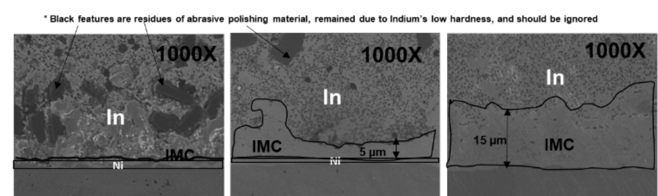

Figure 8. Cross section images of indium- Cu/NiAu interface after a) initial indium reflow, b) 1 time of BM reflow, and c) 3 times of BM reflow

RESULTS AND DISCUSSION

CONCLUSION

This work examines the performance of indium as TIM for BGA packaging. When a liquid flux is applied to activate the indium surface, excessive voids form during subsequential high temperature reflows, which are necessary for BGA packaging. A new generation of indium TIM with a protective layer is introduced in this research. This category of indium TIM does not require liquid flux to activate and wet the substrate. Moreover, even after subsequential high temperature reflows, it shows a significant reduction in voids. IMCs will form at the interface of In-Cu/NiAu during multiple reflow steps. While the IMC bond is developing, Au and Ni are consumed. Depending on reflow process parameters, a sufficient Ni layer thickness is required to maintain a uniform defect-free bond at the joint.

REFRENCES

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