IMPACT OF THERMAL LOADING ON THE STRUCTURAL INTEGRITY OF 3D TSV PACKAGE

Subramanian R Gowthaman, B.E., Unique Rahangdale, B.E., and DerejeAgonafer, Ph.D.
The University of Texas at Arlington
Arlington, TX, USA
subramanian.ramachandrangowtham@mavs.uta.edu;
unique.rahangdale@mavs.uta.edu; agonafer@exchange.uta.edu

ABSTRACT
Today, there is a revolution in going for miniaturization in size of electronic packages. More thinner, lighter and complex packages are in use for almost every electronic device. This initiation was taken to the next level and gives us a whole new ideology called 3D packaging. Currently, 3D packaging is the on-going research in almost all the electronic packaging related industries. 3D package uses Through Silicon Via (TSV) technology that gained momentum in the development and helped packaging system for significant miniaturization and power reduction, which result in increased performance. However, the reliability assessment is needed to evaluate the critical areas in TSV based 3D ICs. In electronic packages, reliability is the most important issue for electronic device manufacturing company and in any research institutes. In this paper, the different types of crack that can happen along the TSV/Si interface has been determined with the study of behaviors of crack. Finite element method is used for the analysis of TSV region and calculation of stress intensity factor (SIF). Stress Intensity Factor (SIF) is a function of applied load, component dimensions and the length of the crack. Analyzing all these functions will help us to give more ideas about crack propagation and thereby help us to take preventive measures.

TSV structure contain silicon and copper which develop stress intensity factor. Comparison of fracture toughness of silicon and developed stress intensity factor is made. Finite element analysis is done to calculate stress analysis due to mechanical effect under reflow conditions, which is important for material characterization, TSV geometry, etc. Interfacial delamination of TSVs may encounter large stress because of the shear stresses that develops at the interface. This creates a relation between crack growth and SIF at the interface. Also the relation between geometry of the package and the crack growth is finally analyzed.

Key words: Crack growth, 3D TSV, SIF

INTRODUCTION
With the technological advancements, the electronics in today's digitalized industry are undergoing integration and miniaturization to become smaller, lighter and denser for greater portability. The chips with more I/O's and state of the art multi-functionality will be going to take of the electronic packaging industry. To meet all the requirements, 3D stacking of chips are developed. At the same time the efficiency, and quality with reduced cost and power loss has to be established. This requires an effective communication between the IC and the electronic systems. Therefore, 3 dimensional integrations have emerged as a boost to electronic packages manufacturing company due to its low cost, small form factor and high performance. TSV technology is used for 3 dimension packages. In TSV package, a thin silicon wafer is drilled with holes, and dielectric SiO_2 is deposited along the inside walls of the holes, and then the hole is filled with copper. One of the issues with TSV is the challenge in removing heat from the system. Otherwise, the CTE mismatch of different material will cause thermal stresses to be developed. Because of the thermal stress there is as keep out zone formed where active transistors cannot be placed. TSV package have some critical stress areas like SiO2/Cu interface, and Silicon . This stresses can develop cracks within the silicon and/or SiO_2 which leads to reliability issues with the package. In this paper, the different types of crack along the TSV interface is determined. Relation between crack location and K1, K2, K3 is obtained. Also, the relation between J-Integral, length of the crack, die thickness and crack size has been calculated. ANSYS 16 bundle is used for modeling and simulation and finite element analysis (FEM) is used to calculate stress intensity factor (SIF) at crack interface.

All crack modeling and semi elliptical crack model has been done in ANSYS 16. Also, the TSV package is modeled on the same software which is simulated to reflow conditions to analyze the various stresses developed within the TSV package using quarter symmetry conditions. The temperature boundary condition subjected to the package is 200 Celsius. Analysis of the TSV silicon/copper interface has been done by sub-modeling technique. It is sliced into equal halves as both are symmetric in shape and will show same property. One half is used for crack modeling and further analysis. The behavior of stress intensity factor and J- Integral is studied by varying die and substrate thickness and also by varying the crack dimensions.

MODEL DESCRIPTION
Global and Sub models
2 die 3-D flip chip along with the TSV has been studied with respect to the crack propagation analysis. The response

of this package after connecting substrate and the chip has also been studied. TSV has a diameter of 10µm including 0.5µm of area covered by dielectric. In order to avoid the adverse effects of silicon efficiency, the TSV is restricted to less than 4 percent. Mirza et al. and Chirag et al. have put forward a novel approach that demonstrates how the reasonable computational time can be maintained There are 3 steps that plays a vital role in simulation. Initially, a global model on the compact scale is formulated and solved. The results from this solution are used to generate boundary conditions to the sub model 1 which is part of the critical region having detailed features (for example practical µ-bump interconnections and TSVs). These boundary conditions are applied on the sub model 2 which is part of the sub model 1. In order to prevent rigid body motions, a center node at the bottom is fixed and normal displacement with respect to the symmetric faces are constrained. Using linear elastic material properties from Pavan et al, all of the materials except copper (TSVs and BEoL) and solder (SAC305) are modeled. Using Anand's viscoplastic model and considering the creep and plastic deformations (representing secondary creep), solder is modeled as rate dependent viscoplastic material. In order to describe the inelastic behavior of lead free solder, Anand's viscoplastic constitutive law has been used. Anand's law has an impact on total of nine material constants A, Q, ξ, m, n, h, a, s_0 , ŝ (all of which are extracted from the curve fitting experimental data) that are used throughout the solder strain-rate and temperature sensitivity.

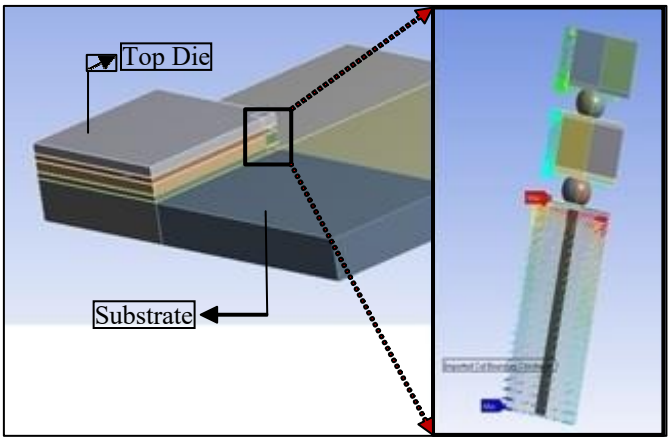

Figure 1. Global Model with Exploded Sub model 1

Table 1. Anand's Constants for SAC305

S. No.	Anand's Constant	Units	Value
1	s_0	MPa	1.3
2	Q/R	1/K	9000
3	A	sec^{-1}	500
4	ξ	Dimensionless	7.1
5	m	Dimensionless	0.3
6	h_0	MPa	5900
7	ŝ	MPa	39.5
8	n	Dimensionless	0.03
9	a	Dimensionless	1.5

Table 2. Anand's Constant for Effective Block in the Compact Model

S. No.	Anand's Constant	Units	Value
1	s_0	MPa	0.15
2	Q/R	1/K	9000
3	A	sec^{-1}	500
4	ξ	Dimensionless	7.1
5	M	Dimensionless	0.3
6	h_0	MPa	5900
7	Ŝ	MPa	3
8	N	Dimensionless	0.03
9	A	Dimensionless	1.5

Crack propagation is placed in different location along the cylindrical silicon die interposer where the TSV and copper passes. In this experiment, silicon and silicon dioxide is covered as the critical area on TSV interface. Therefore, the crack is modeled successfully along the silicon die/Cu interface. This is the prominent region for critical stresses acting where more chances of crack to be develop.

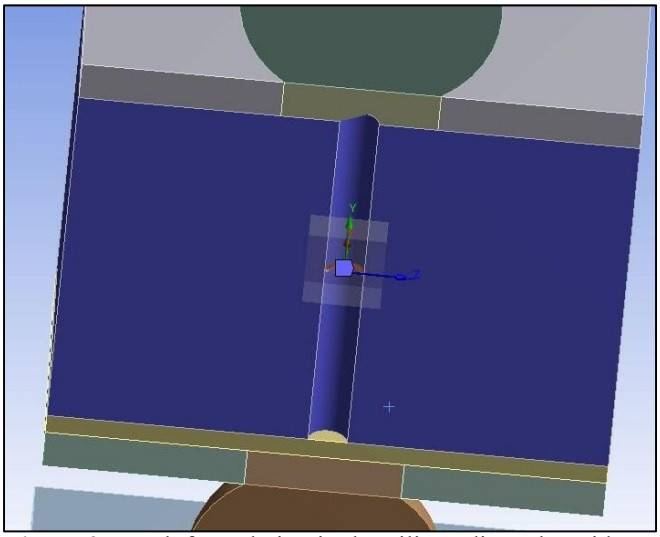

Figure 2. Crack formulation in the Silicon die at the mid-section of Sub model 2

All modeling and formulation of radial horizontal crack for the TSV package are done using ANSYS 16 bundle. The tetrahedron mesh profile is used here and only semi elliptical cracks can be model on the exterior surface using the software. The global model as a compressive model is subjected to same reflow conditions. The sub model 1 has been cut into two halve and simulation is done with same reflow conditions. The crack has been modeled in the sub model 2 which is one of the symmetrical halves of sub model 1. The sub model 2 was again subjected to the same reflow condition with importing cut boundary constraints from the sub model 1.

In Figure 6, from the plot between K3 and the crack location, the top and bottom portions of the TSVs are more susceptible to mode 3 fracture, as the value of K3 is lower in the middle region.

10 divisions with equal space have been taken for simulation of crack where the total edge length of TSV is 95 µm. All the simulations are done along the length of TSV in sub model 2 with equal division of 9.5 µm. When it is attached to the substrate, reflow condition is taken for thermal loading in 3D TSV package from 200°C to room temperature (for Pb-free SAC305 Alloy). The plot for relation between stress intensity factor (SIF) (i.e. K1, K2, K3) and crack location have been shown in this paper. Also, the relation between crack size, crack length and J-integral is shown in the plot. The results show that the TSV area is much affected by mode 1, mode2 and mode 3 cracking. To avoid radial crack, K should be less than Kc, i.e. K<Kc where Kc is fracture toughness of silicon.

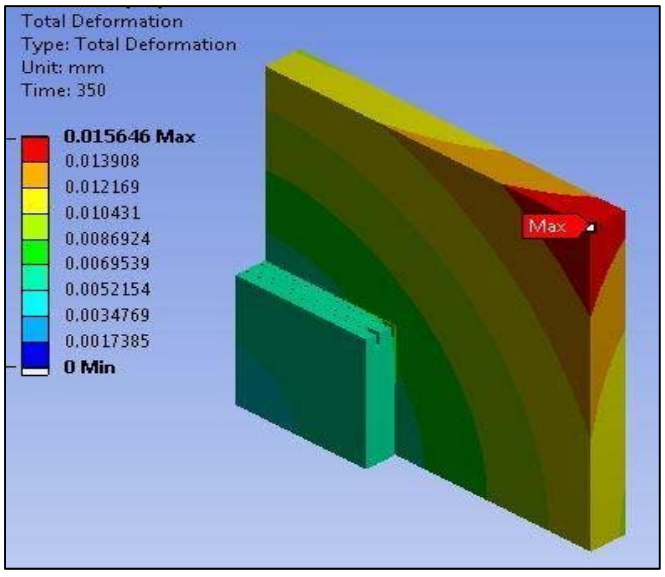

Figure 3. Deformed Global Model

Simulation and Validation

The analysis result shows that the normal stress (in Z direction in our case) is positive across the middle area of the silicon/ copper interface. The stress distribution data is obtained after simulating under reflow conditions. The middle area of TSV is influenced to Mode 1 fracture, which is determined from the plot shown. The value K1 increases at the start and then decreases. It is positive at the middle region (Figure 4).

Crack on mode 2 is predominant on the top region of the interface (Figure 5). In Figure 6, from the plot between K3 and the crack location, the top and bottom portions of the TSVs are more susceptible to mode 3 fracture, as the value of K3 is lower in the middle region.

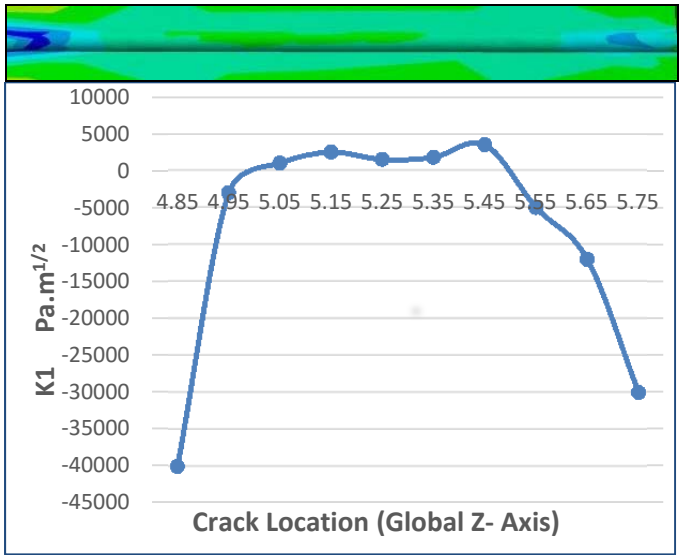

Figure 4. Silicon die/Cu stress distribution with K1 plot

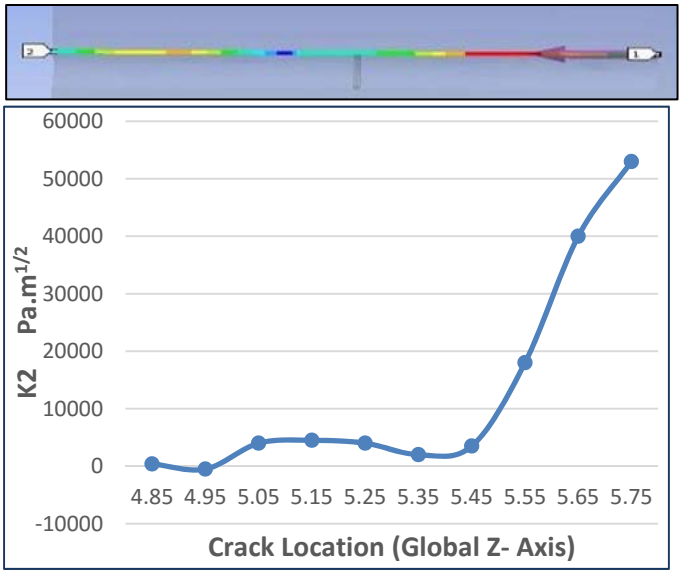

Figure 5. K2/Crack location plot

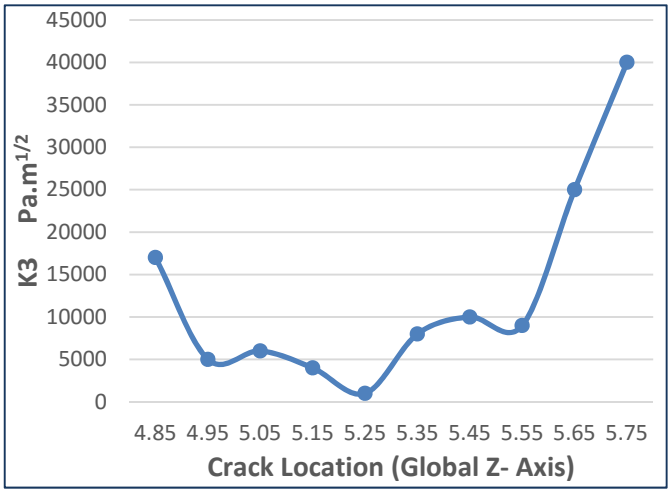

Figure 6. K3/Crack location plot

J-Integral

J-integral is used to calculate the strain energy release rate per unit fracture surface. It is not path-independent of while loading elastic-plastic material. Rice,J.R., 1968, showed that the J integral is a path independent line integral and it represent the strain energy release rate of non-linear elastic materials. The value of J is determined by calculating the area under load versus deflection curve.

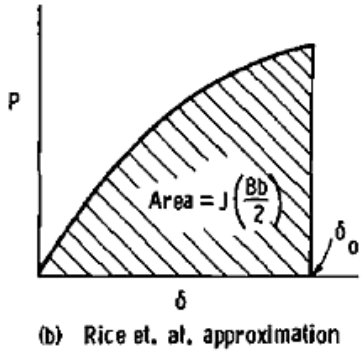

Figure 7. Load vs Deflection

Relation between J-integral and different dimension parameter

The study of crack behavior with change in different dimensional parameter is studied in this paper. This plot incorporate variation of J- integral with substrate thickness, die thickness, crack size and length of the crack. The analysis showed the significant change in J- integral values as die and substrate thickness increases.

The J- integral have relationship with substrate thickness that causes crack formation. The substrate thickness was varied from 0.2mm to 1mm with 0.2mm intervals and the corresponding J-integral value is noted. The data is plotted in graph and it has been observed that the value of J-integral decreases as the value of substrate thickness increases. After a certain limit the J-integral value starts to increase at a lower rate as showed in Figure 8.

Similarly, the top die variation has been done by varying the thickness in equal increments of 0.1mm and the corresponding J- integral is noted. The value of J-Integral decreases drastically upto a certain limit and then remains the same even when the top die thickness increases as showed in Figure 9.

Table 3. Variation of J-integral with length of crack

Length of the crack (microns)	J-integral (J/mm²)	Increasing Percentage
1	.12303	
5	.38334	211.58%
10	0.90246	135.42%
15	1.2012	33.10%
20	1.5078	25.52%
25	1.8385	21.93%
30	2.0917	13.77%
35	2.3412	11.93%

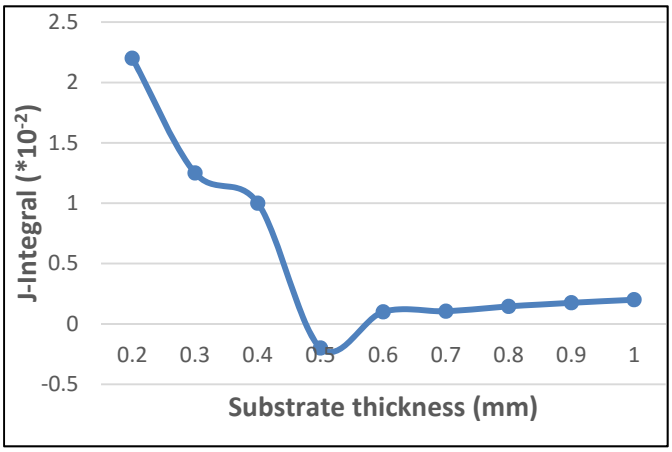

Figure 8. J-Integral vs substrate Thickness Plot

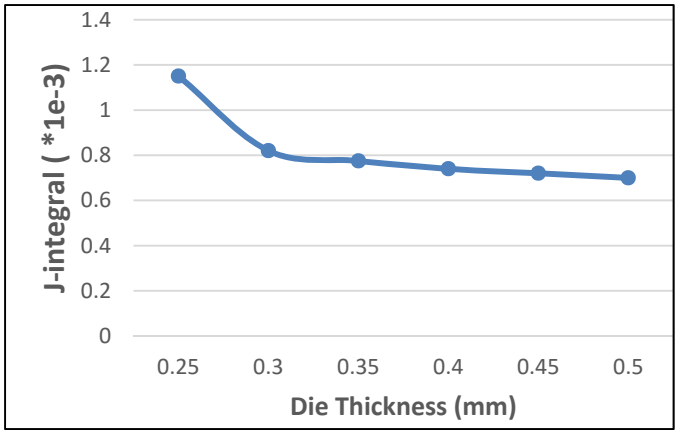

Figure 9. J-Integral vs Die thickness Plot

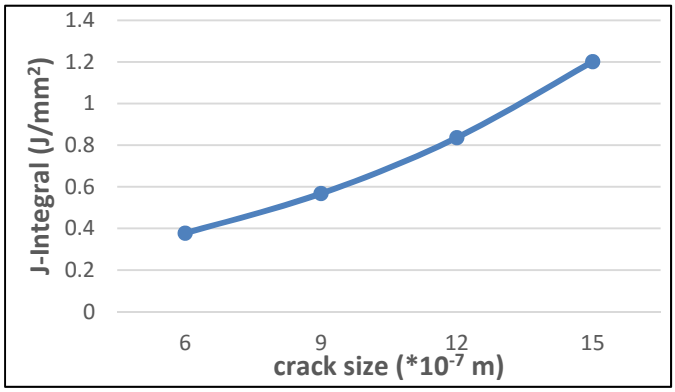

Figure 10. J-Integral vs crack size Plot

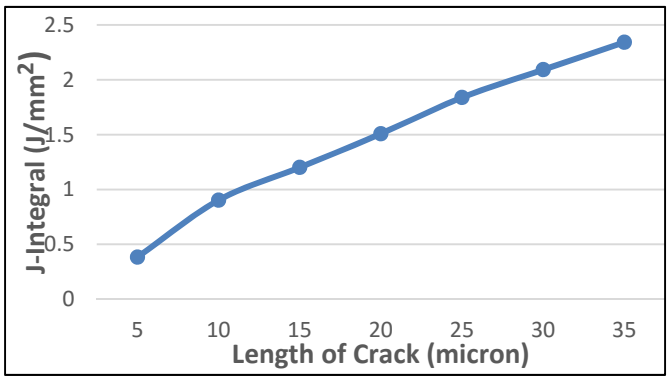

Figure 11. J-Integral vs length of crack Plot

The radius of the crack is increased from 1 micron to 35 microns with 5 microns interval and the corresponding J-integral is noted. The variation of the values of J-integral with respect to length of crack is tabulated in Table 3. The J-integral increases as the length of crack increases. The plot to given data is shown in Figure 11.

Table 4. Variation of J integral with crack size

Crack Size (E-07m)	J-integral (J/mm²)
3	0.29643
6	0.37719
9	0.56732
12	0.83614
15	1.2012

The crack size increase from 0.3 microns to 1.5 microns in the interval of 0.3 microns and the corresponding J- integral is noted and tabulated in Table 4. The variation of J- integral with crack size is shown in Figure 10. The J-integral increases as the crack size increases.

RESULTS AND DISCUSSION

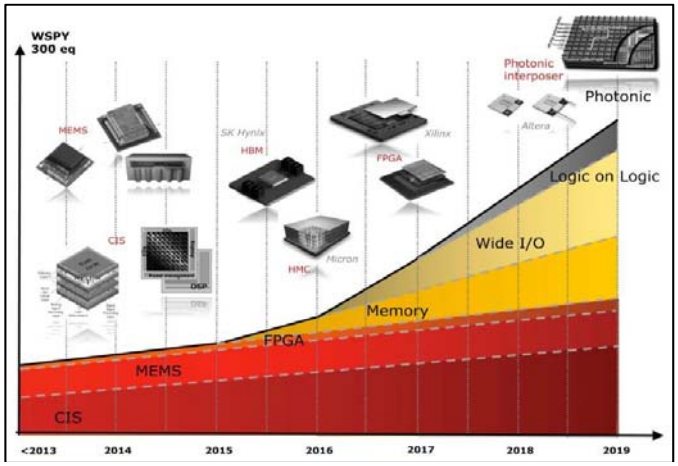

Figure 12.3D TSV Wafer breakdown by Application [4]

Almost all electronic devices deal with thermomechanical condition. The mismatch in material properties like CTE, cause stress concentration. In TSV technology, the mismatch in CTE cause stress concentration on the interface between copper or/and silicon dioxide, the dielectric and TSV.

As it is mentioned in this analysis, the mismatch in the material property may cause the crack to propagate in the critical areas where magnitudes of K1, K2, and K3 are higher. The focus of this research is to study the crack propagation when the TSV region is subjected to thermomechanical stresses and to show the effect on variation of J-integral with the variation of crack dimensions.

All the results are in congruence with the hypothesis that "if the geometry of the crack increases with respective to the geometry of the model, then the J-integral value also increases".

CONCLUSION

The variation of radial crack or crack propagation along the length of the silicon die has been successfully studied, through the TSV passage. The crack is modeled successfully and checked for different dimensions of crack. The cut boundary condition from the global model and sub model where used for simulation. The variation of J –integral value is used in calculating strain energy release rate per unit fracture surface and is determined with respect to crack size, die – substrate thickness and length of crack. The variation of crack length and size has also been successfully leveraged to investigate its effect on stress distribution and found that it is directly proportional to J- integral, whereas the relation between J-integral and die-substrate thickness shows an inversely proportional relational property upto certain limit of thickness.

REFERENCES

[1] Ramm P, Wolf, MJ, Klumpp A, et al, “Through silicon via technology – processes and reliability for wafer-level 3D system integration”, 58th Electronic Components and Technology Conference, Orlando, FL, pp.841-846,2008.

[2] Khan N, Rao S, Lim S, et al, “Development of 3D silicon module with TSV for system in packaging”, 58thElectronic Components and Technology Conference, Orlando, FL, pp.550-555, 2008.

[3] Lau JH. Overview and outlook of through-silicon via (TSV) and 3D integrations. Micro electron Int 2011; 28:8–22.

[4] 3DIC & 2.5D TSV Interconnect for Advanced for Advanced Packaging 2014 Business Update report, Yole Development, July 2014.

[5] E. J. Cheng, Y.L. Shen, “Thermal expansion behavior of through-silicon-via structures in three- dimensional microelectronic packaging”, 2011.

[6] P. Rajmane, F. Mirza, et al, “Chip Package Interaction to Analyze the Mechanical Integrity of a 3-D TSV Package”,2015.

[7] Selvanayagam, CS; Lau, JH; Zhang, XW, et al., “Nonlinear thermal stress/strain analyses of copper filled TSV (through silicon via) and their flip-chip microbumps”, 58th Electronic Components and Technology Conference, Orlando, FL, pp.1073 1081, 2008.

[8] F. Mirza, “Compact Modeling Methodology Development for Thermo-Mechanical Assessment in High-End Mobile Applications” - Planar 3D TSV Packages, Arlington, TX,2014.

[9] Karmarkar AP, Xu X, Moroz V. Performance and reliability analysis of 2D integration structures employing through silicon via (TSV). In: Proc IEEE 47. Annual IntReliab Phys Symp; 2009. p. 682–7.

[10] Reiske R, Landgraf R and Wolter KJ, “Novel method for crystal defect analysis of laser drilled TSVs”, 59thElectronic Components and Technology Conference, San Diego, CA, pp.1139- 1146, 2009.

[11] C. Shah, F. Mirza and C. S. Premachandran, "Chip Package Interaction(CPI) Risk Assessment On 28nm Back End Of Line(BEOL) Stack Of A Large I/O Chip Using Compact 3D FEA Modeling," in EPTC, Singapore, 2013.

[12] Kuo TY, Chang SM, Shih YC, et. al, “Reliability tests for a three dimensional chip stacking structure with through silicon via connections and low cost”, 58th Electronic Components and Technology Conference, Orlando, FL, 2008.

[13] J. R. Rice, “A path independent integral and the approximate analysis of strain concentration by notches and cracks”.

[14] N. E. Dowling and J. A. Begley,” Fatigue crack growth during gross plasticity and the J-integral”.

[15] Mohammed Shahid Ali, “Estimation of fracture mechanics parameters in 3D TSV package during chip attachment process”.