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Basic PCB Level Assembly Process Methodology for 3D Package-on-Package

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Abstract
The motivation for developing higher density IC packaging continues to be the market and the consumers' expectation that each new generation of products furnish greater functionality. The miniature IC package evolution began with the development of chip-scale and die-size package technology. These miniature IC package innovations proved ideal for portable and hand-held electronic applications. To address the need for even more functionality without increasing their products size, a number of companies have adapted various forms of multiple-die 3D packaging. A majority of these early multiple function devices relied on the sequential stacking of die elements onto a single substrate interposer. Because the wire-bonding of multiple tiers of uncased die is rather specialized and the die used may have had relatively poor wafer level yields or were not always available in a pre-tested (KGD) condition, overall manufacturing yield of the stacked-die packaged devices have not always met acceptable levels. A key advantage of the package-on-package process is that each layer of the package can be pre-tested before joining. This capability greatly improves the overall manufacturing yield and the functional reliability of the final package assembly is assured. The information furnished in this paper will focus PoP package standards,, substrate design criteria and assembly methodology for efficient in-line assembly processing of vertically stacked IC package elements.

Introduction
Solutions for packaging multiple die elements in a single package outline have evolved rapidly. Vertically stacking several semiconductor die on a single semiconductor package substrate proved efficient for a number of high density memory applications, however, when mixing some of the newer multiple function processor and controller products with the more mature high yielding memory die elements, the overall package yield did not always meet expectation. A solution that has proved to be more efficient is a package-on-package (PoP) methodology designed to vertically combine fully packaged and pre-tested discrete logic and memory on separate array configured package substrate levels that are designed to align and mount on top of one another typical of the example shown in Figure 1.

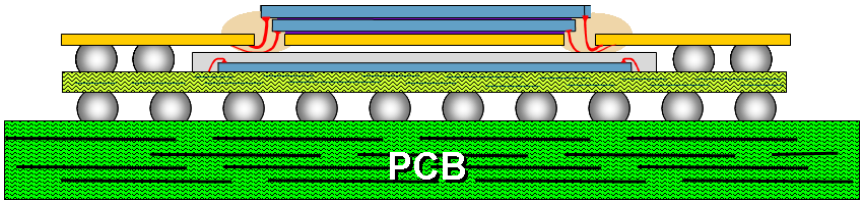


Figure 1. Package-on-Package example combining logic and memory

Package stacking is proving to be ideal for a variety of applications requiring greater functionality, high performance and a smaller footprint: Stacking pre-tested package sections enable a high degree of flexibility for designers, allowing virtually any combination of memory to be combined with any logic chip set. Combining discrete logic and memory packages in this vertical configuration not only saves space on the circuit board, it typically reduces pin-count, simplifies system integration and enables enhanced performance. A number of products are already taking advantage of this multiple die packaging solution include Wireless handsets, Digital cameras, portable game players and GPS products

Wireless handset designers in particular are faced with many challenges. They are tasked with providing more and more features while addressing requirements for decreased product size and weight. Because many of the stacked PoP memory products are commonly furnished with a consistent footprint and pinout, users can easily configure variations that meet different product applications or incorporate new Flash, SDRAM, or other devices as they are introduced.

Package-on-Package Design Standards
The JEDEC Publication 95-4.22 Package-on-Package (PoP) design guide standard specifically defines a multiple die configuration that has at least two micro-electronic packages assembled in a vertical stack. Although package stacking can be

done with a variety of package styles, this design guide focuses only on utilizing physical parameters previously established for the Fine-pitch Ball Grid Array (FBGA) package family to create the stack. Typical of the FBGA, the lower package of the stack includes a ball or bump contact array on the lower surface for PCB mounting. In addition, a pattern of metalized lands are provided on the top surface of the packages flange for joining the second level package section. The JEDEC design guide also furnishes recommendations on land geometry and ball diameters needed to facilitate the stacking process. The ball pattern of the upper package, for example, is designed to facilitate the connection between the upper and lower package sections (see Figure 2).

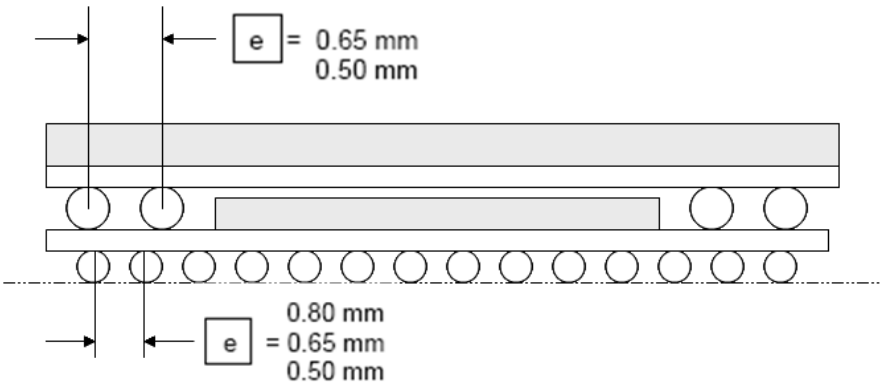


Figure 2. JEDEC PoP profile example

From the profile detailed above, ball diameter and contact pitch variations are adjusted to accommodate the requirements of specific applications. The larger ball diameter on the upper package for example, will provide additional clearance height that may be needed to avoid interference during assembly between the lower and upper section of the PoP device. The JEDEC guideline also recommends that, wherever possible, dimensions common to the established FBGA package family be used and dimensions specific to package stacking be identified. Additionally, the FBGA Design Requirement standard defines the symbols, definitions, algorithms, and specified dimensions and tolerances for FBGA packages with square outline that are most compatible for PoP applications. All product outlines submitted to JEDEC for registration must have metric dimensioning per JEDEC Publication 95 (JEP95), Sub-Section 3.0, SPP-003, and adhere to the geometric dimensioning and tolerance methods defined in ASME Y14.5M-1994.

Package Stacking Process

When the PoP device is furnished to the user pre-joined, the package can be handled and mounted onto the circuit using conventional SMT soldering processes. These products are furnished in standard carrier tray as a fully tested package unit. Some users will insist that the sections be furnished as separate pre-tested packages ready for joining during the board level assembly process. The later version enables flexibility in system configuration and supply chain management. In either case, these devices are normally compatible with existing surface mount assembly process methodologies. In regard to soldering, the base package and top package units are typically furnished with alloy spheres that are compatible with most lead-free solder compositions. If the user chooses to perform the joining of the package sections during board-level assembly, they will need to consider how the PCB land patterns are prepared for soldering and assembly machine flexibility.

Depositing solder paste on a circuit board is most commonly performed using a stencil printing process providing solder to all component attachment sites with a single process step, however, mounting the upper section will require a different strategy. Due to the physical profile of the base package unit, depositing solder paste on attachment sites distributed on the narrow top edge of the base unit is somewhat of a challenge. Stencil printing solder paste at these contact sites is really not practical, but component suppliers have successfully adopted several alternative methods to accommodate attachment of the upper package section. This includes solder paste and flux paste dispensing at each contact site, solder flux-dip transfer and solder paste-dip transfer to the upper package section before placement on top of the lower package section.

Package Stacking

A number of solder suppliers offer dip-transfer compatible flux and a combination of flux and solder in a paste like material. The Indium Corporation for example, offers a halogen-free solder paste material (Indium9.88-HF) that is available in two alloy configurations, Tin/Lead eutectic (63Sn/37Pb) and SAC 305 (96.5Sn/3.0Ag/0.5Cu). In preparation for the dip-transfer process, the material is deposited into a shallow reservoir and maintained at a precise level using a doctor-blade mechanism. Typical package-on-package applications only require 25-45% of the sphere height to be coated with flux or solder paste. A number of automated assembly systems are available that have been configured to accommodate 3D package stacking and

have included dip-tray stations between the package pick-up location and the circuit board. This feature was originally intended for flip-chip assembly processing but it works just as well for PoP applications as shown in Figure 3.

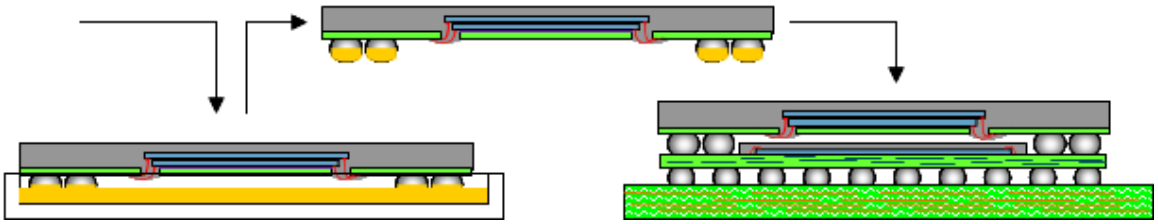


Figure 3. Package-on-Package assembly process

The peak reflow temperature will vary, depending on the specific solder alloy composition selected. Solder suppliers recommend a short preheat (140-150°C for 63Sn and 150-160°C for SAC305) for less than 45 seconds be used to reduce any solder balling caused by excess paste. Solder suppliers state that the reflow solder profiles should be a linear ramp at 1 or 2°C per second up to 20-30°C above solidus temperature, the minimum time above liquidus should be 20 seconds and followed by a rapid cool down to reach the solidus state. To monitor this procedure, the newer generations of precision pick and place systems are equipped with bottom focused digital cameras that, when programmed, can detect missing solder ball contacts and/or identify a contact without the correct volume of flux or paste coatings. When solder paste is employed, users note that additional care must be taken to avoid excessive paste residues on the bottom surface of the package as this may cause solder bridging defects.

The examples shown in Table 1 represent a few suppliers offering flux paste materials formulated with a viscosity suited for the dip transfer process.

Table 1:
Dip transfer flux paste material examples

Manufacturer	Type	Water Clean
Indium	WS-364	Yes
Amtech	WS-4200-LFTF	Yes
Alpha	WSX-FD	Yes

Although water soluble materials are shown in the table, no-clean fluxes are also available.

For optimum performance the manufacturer recommends that the solder paste syringes and cartridges be stored tip down at ≤10°C for maximum shelf life. Storage temperatures should not exceed 30°C for more than 4 days. The material should be allowed to stand for at least 4 hours at room temperature before using. Once removed from cold storage, the solder paste in a sealed syringe may remain at room temperature for up to seven days before usage and during usage. However, once outside the syringe, its working life is estimated to be no greater than 8 hours, and may be less under high temperature (>25°C) and humidity (>70%RH) conditions. Furthermore, the paste should not be subjected to multiple cold/heat cycles because viscosity can change and flux separation may occur. A number of materials have been formulated for no-clean applications, and can be left in place on the final package, however, when necessary, any flux residues that may impede the uniform flow of underfill material can be removed by using a commercially available flux cleaner.

Post Assembly Process Evaluation

One of the challenges suppliers of the PoP devices were faced with was managing the CTE mismatch and modulus variation of the dissimilar materials within a package. Although the PoP device will experience several levels of temperature exposures during assembly processes, the plastic based components are expected to meet acceptable planarity and flatness requirements. The JEDEC design guide document recognizes the relatively wide TCE differences between the die element and resin based materials used in the package assembly process. The standard, however, does not specifically define a 'flatness' criteria but it does, however, establish a parallelism tolerance of 200 microns for controlling the orientation of the top surface of the package with respect to the seating plane. The planarity limit of the seating plane contact features must be within 100 to 120 microns (depending on the ball diameter used). Even so, the tandem package configuration may be prone to some degree of package warp during the board level assembly process due in part to the physical variation between the resin based multilayer

circuit board material and the relatively thin resin based package substrate materials. The guidelines caution the user that, if this warp condition is excessive, it can cause random solder defects that may compromise product reliability or prevent proper functionality.

Primary markets for the PoP devices are miniature portable products where package outline, profile height and package warp must be minimized. The substrate warping issue has plagued the multi-level package products throughout their relatively brief history. Manufacturers recognized the negative warp affect of the outer edge area of lower package interposer. During the package-to-board assembly process, if the base (or lower package) substrate flexes downward at its edge, the solder ball contacts mating with the host PC board can collapse to the point of merging together. Likewise, if the second level package substrate warps in the opposite direction of the lower package the solder interface will elongate and possibly separate. Additionally, package assemblers have noted that most of the upper level packages will have two or more die, further complicating the physical dynamics of the joining process. The accumulated die thickness along with the physical support of a high temperature mold compound should minimizes the warp condition on the upper package section, however, the mold compound furnished on the lower package only helps to minimize warping in its mid-section. The unsupported, relatively thin perimeter flange area, the portion of the package that is configured to join with the upper level package is not restricted and is more prone to warping during the solder joining processes.

Providing Physical Reinforcement

Many of the ball grid array configured PoP products are targeted for the commercial wireless handset market. Because these handsets are subjected to various degrees of physical shock, vibration and thermal gradient extremes, some manufacturers of these products will physically stabilize the array packages with an epoxy resin underfill. The liquid underfill material is typically dispensed at the package edge and, by capillary action, flows under the device to furnish a mechanical bond between package and PC board. There are several different types of underfill used in the electronics industry. The most commonly used underfill compounds are referred to as ‘snap cure’, ‘low profile’, ‘high performance’, and ‘reworkable’: Examples for a number of suppliers and commercially available underfill materials are compared in Table 2.

Table 2:
Underfill material sources

Manufacturer	Type	Attributes
Hysol	FP4580	Low stress liquid epoxy
Namics	U8439-1	Low stress, High moisture-resistance
Protavic	ANA 10199 R	Fast flow, fast cure, reworkable
Lord Corp.	ME-532	Fast flow, high performance
Masterbond	EP3RR-1UF	Rapid cure, excellent flowability

To reduce voiding and ensure proper flow and adhesion of the underfill material, the surfaces of the PC Board and package substrate must be free of any flux residues. In addition, component suppliers warn users that most of the materials used for both underfill or molding are prone to varying degrees of moisture absorption.

Addressing Future PoP Applications

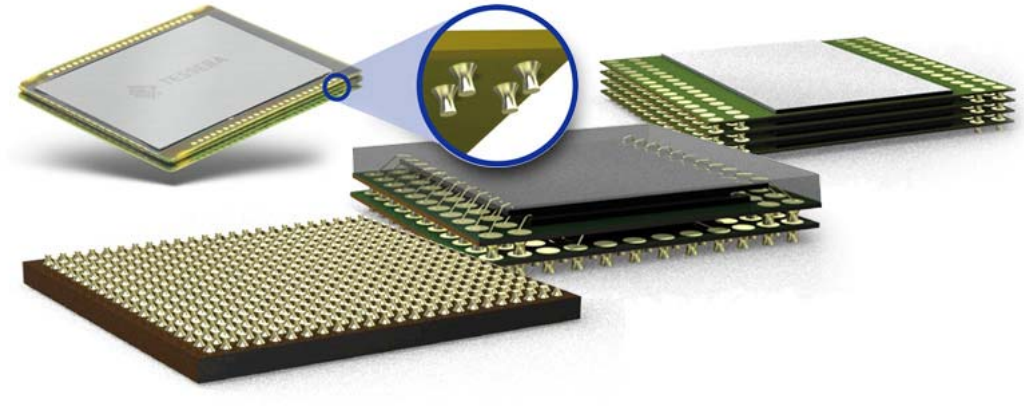
Looking to the future, users are expecting following generations of PoP to furnish significantly greater functionality. Due to the increased complexity of the logic die elements and the demand for greater memory capacity, more contacts will be needed for both the upper package section and lower package section. For many of these applications the OEMs would like to limit the outline to 12 mm x 12 mm (10 mm x 10 mm would be even better). The current JEDEC design guide standard defines a minimum contact pitch of 0.50 mm allowing a maximum I/O for a 12 mm square configuration of 529 and only 361 I/O for a fully populated 10 mm square package. To meet the I/O density for the next generations of mixed function 3D packaging, many companies are anticipating the adoption of 0.4 mm and even 0.3 mm contact pitch.

Although widely used for single die wafer level (WLCSP) and flip-chip (FC) applications, the finer pitch for an alloy ball or bump contact configurations on PoP applications are proving to be very difficult to manufacture. Some companies have found limited success by printing and reflowing solder onto the ultra-fine pitch contact sites but profile uniformity of the contact features do not always meet the established criteria for planarity. Avoiding the need for underfill is also a goal for many companies manufacturing products in high volume. Until this process stage, everything is running hands-free and smoothly through a series of conveyor transfer systems, from package placement to reflow and cleaning. The assembly is then transferred to a dispensing station for applying the underfill material and, for some materials, a curing cycle that could

be as long as one hour. Add to that, the detection and correction of any solder process defects or package removal and replacement after underfill is applied may be difficult or not practical.

Ultra-Fine Pitch PoP Solution

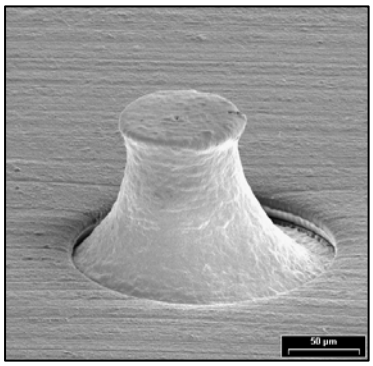
Forecasting the requirements for 'next generation' products requires broad knowledge of the market trends and an understanding of fabrication process capabilities and limitations. Analysts predict that although the PoP configuration has a very secure position in the industry near-term, the newer generations of silicon products will be far more complex and will require a significantly higher pin-count and finer contact pitch than the current vertically configured FBGA package can handle. A viable solution is being offered to provide finer pitch and higher contact density for the PoP package applications. A unique substrate interposer fabrication process has been developed by the San Jose California based IP company *Tessera*, that furnishes solid raised copper contact features for both package stacking and board mounting in place of the ball or bump contact features. The name coined by the company to best describe this unique contact profile is 'µPILR™", providing significantly smaller contact feature and finer pitch typical of those shown in Figure 4.



Example source: Tessera

Figure 4. Package-on-Package examples with 0.40mm pitch µPILR™ contacts.

When comparing the µPILR contact profile to the more common solder ball connections, the contact geometry is significantly smaller in both diameter and height, enabling a much lower finished package profile. The solid copper core contact illustrated in Figure 5 is slightly tapered in shape and coated with a nickel/gold (ENIG) alloy that is compatible with either eutectic or lead-free soldering processes.



Example source: Tessera

Figure 5. Solid copper core µPILR contact profile.

Circuit board assembly of the 0.40mm pitch µPILR package-on-package device is very typical of most surface mount processes beginning with solder paste printing, pick-and-place and reflow soldering. The stencil developed for printing the solder paste on the PCB specifies a 100 micron thick stainless steel foil with laser ablated 270 micron square apertures. Because of the very small stencil aperture, the recommended solder paste used for this application is a Type 5 powder size. Precise placement of the 0.40 mm pitch components is critical as well. When placing ultra-fine pitch array devices, machine placement accuracy should be in the range of +/- 20 microns to assure a reasonably uniform solder fillet at all contact sites.

In the course of developing µPILR package technology, insight was gained into the relevance of various SMT factors to board-level robustness and reliability. One of the benefits of this high-density package substrate structure is the ability to reduce interconnect solder volume and tailor the solder shape to allow for closer spacing of interconnects between package and board. The µPILR package-on-package device has the advantage of an extended solder wetting plane provided by the package contacts making it less susceptible to solder defects caused by the warping, most typical of the BGA configured devices. Also, the µPILR package does not require the post assembly application of underfill for mechanical stability or reinforcement. This is due to the solid copper pins providing crack stop reinforcement against solder fatigue cracks resulting from mechanical shock or thermal cycling. Reliability tests have shown the µPILR PoP to outperform the BGA PoP package and exceed customer standards in drop testing and temperature cycling by 3x to 8x without underfill.

Conclusion

Package-on-Package technology has proved to be a practical solution for a number of high-performance, system-level applications. Whether the IC package sections are manufactured within a closed (in-house) environment or supplied from outside sources, quality and integrity of the end product is paramount. However, source and configuration control and material tracking throughout the life of the product are also a concern. Because each package section of the PoP component has been electrically tested before PCB mounting, the user can be assured that the multiple die products will meet all performance criteria without compromise. Even when IC package sections are furnished by differing offsite suppliers, the logic device supplier is responsible for assembly and test for the logic section, and the memory manufacturers will be responsible for assembly and testing of the respective memory section.

In regard to future applications, because the µPILR package enables a much finer pitch, a significantly higher number of contacts can be provided on both upper and lower package sections without increasing package size. In addition, the package assembly process utilizes an existing and mature manufacturing infrastructure allowing technology transfer to multiple sources of supply. In regard to package reliability, the µPILR package structure has demonstrated excellent board-level durability, meeting or exceeding industry recognized thermal cycle and drop-shock requirements for lead-free soldering without using underfill or other reinforcement methods.

Because PoP designs are becoming more complex and the number of PoP interconnects between top and bottom packages are increasing, there is a growing demand for finer pitch PoP technologies capable of delivering 0.4mm or even 0.3mm pitch. There are limited options available that can meet this demand, but a growing number of semiconductor and OEM companies have concluded that the µPILR PoP is one such solution.

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