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Packaging Technology and Design Challenge for Fine Pitch Micro-Bump Cu-Pillar and BOT (Direct Bond on Substrate-Trace) Using TCNCP (Thermal Compression with Non-Conductive Paste Underfill) Method

***MJ (Myung-June) Lee – Altera Corporation**

**SungSoon Park, DongSu Ryu, MinJae Lee – Amkor Technology Inc.

***Hank (Hajime) Saiki, Seiji Mori, Makoto Nagai – NTK Technologies, Inc

*Altera Corporation, 101 Innovation Drive, San Jose, CA 95134 U.S.A.

mjlee@altera.com

**Amkor Technology Korea Inc. 280-8, 2-ga, Seongsu-dong, Seongdong-gu, Seoul, Korea

***NTK Technology, 3979 Freedom Circle, Suite 320, Santa Clara, CA 95054 U.S.A.

hsaiki@ntktech.com

ABSTRACT

The companies writing this paper have jointly developed Copper (Cu) Pillar micro-bump and TCNCP(Thermal Compression with Non-Conductive Paste) technology over the last two+ years. The Cu Pillar micro-bump and TCNCP is one of the platform technologies, which is essentially required for 2.5D/3D chip stacking as well as cost effective SFF (small form factor) package enablement.

Although the baseline packaging process methodology for a normal pad pitch (i.e. inline 50µm) within smaller chip size (i.e. 100 mm^2) has been established and are in use for HVM production, there are several challenges to be addressed for further development for commercialization of finer bump pitch with larger die (i.e. ≤50µm tri-tier bond pad with the die larger than 400mm^2).

This paper will address the key challenges of each field, such as the Cu trace design on a substrate for robust micro-joint reliability, TCNCP technology, and substrate technology (i.e. structure, surface finish). Technical recommendations based on the lessons learned from a series of process experimentation will be provided, as well. Finally, this technology has been used for the successful launching of the company FPGA products with SFF packaging technology.

Keywords

Copper pillar, Micro-bump, TCNCP (Thermal Compression and Non-Conductive Paste), SFF (Small Form Factor), RDL (Re-Distribution Layers), UBM (Under Bump Metallization), SAM (Scanning Acoustic Microscopy), DFM (Design for Manufacturing), DR (Design Rule), POR (Plan of Record), BOM (Bill of Material), iSRO (Isolate Solder Resist Opening)

1. Introduction

As Copper (Cu) pillar bump technology becomes more mature, it is gradually taking the place of the conventional solder base bump in flip chip interconnections, especially in devices requiring a finer bump pitch less than 150~130µm down to 40µm. A typical Cu bump is composed of Cu column (pillar) base and solder cap. A columnar Cu base can be a circular or ovular shape, and the solder cap, typically composed of a Tin/Silver (SnAg) solder alloy, which is plated on top of the Cu column. Several motivating facts that drives Cu bump over solder bump are the superiority of mechanical endurance, electrical performance, and the packaging assembly manufacturability for finer pitch devices.

The mechanical durability of Cu helps to improve the bump reliability from joint fatigue failure. Decreasing the bump pitch triggers a higher risk of electro-migration by increasing the density of the electrical current and thermal energy in the flip chip interconnection, but the Cu bump is enough to compensate for the weakness of the solder bump. The finer pitch scaling capability of the Cu bump can also help to reduce the bump bridge issue at the flip chip attach manufacturing process compared with the solder bump. Another favorable output from the implementation of the Cu bump is satisfying EU and Industry ROHS-6 requirements by achieving Pb-free bump compliance with minimal effort.

Another field in which the fine pitch Cu-pillar technology is gradually replacing is the chip-to-package interconnection using wire bonding technology. Dominant among several challenges on wire bonding interconnection are the limitation of physical-mechanical coverage and electrical performance. The physical-mechanical limitation comes from the complicated wire bond

design rule (i.e. wire angle, length, loop control, bond pad, and finger dimension per wire size) which results in a limited IO density of wire bond devices and gates to achieve package miniaturization. It is a well known fact that enabling the Fine Pitch Cu Pillar Technology is the most effective way of solving these issues and challenges while achieving a higher IO density within the smallest form factor package possible and improving electrical performance. This paper will mainly discuss the challenges on packaging process technology: how to engineer a Cu pillar structure, how to decide substrate structure (i.e. bond on trace) and surface finish, and how to establish a manufacturing friendly assembly process (i.e. TCNCP versus mass-reflow).

2. Package Structure, Bumping and Assembly Process Flow

Conventional FCBGA and chip scale fcCSP packages consist of a silicon chip, bumps (solder or Cu pillar), capillary or molded underfill encapsulant, a thermal lid, an organic laminated substrate (Figure 1).

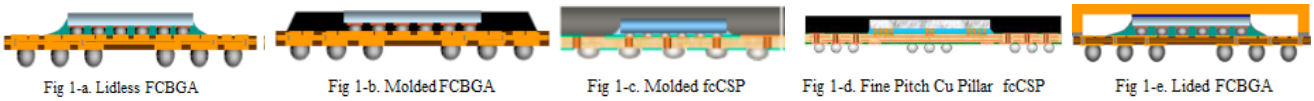


Fig 1-a. Lidless FCBGA | Fig 1-b. Molded FCBGA | Fig 1-c. Molded fcCSP | Fig 1-d. Fine Pitch Cu Pillar fcCSP | Fig 1-e. Lided FCBGA

Figure 1. FCBGA and fcCSP Packages

In order to put bumps on silicon chips, it is required to layer UBM (under bump metallization) over either Aluminum or Copper metal pads mainly for the component reliability and performance. Typical UBM stacks comprise of two to four layers of certain metals, of which the most commonly used are Titanium, Copper, Tungsten, Palladium, and Nickel. The thickness of the metal pad and each metal layer in the UBM stack vary according to the silicon and bump design, as well as the product application. RDL (re-distribution layers) using Cu traces are often used to apply Cu pillar bump for a silicon die designed for wire bonds. The typical structure and process flow of RDL, Bump and Assembly is shown in Figure 2 and Figure 3.

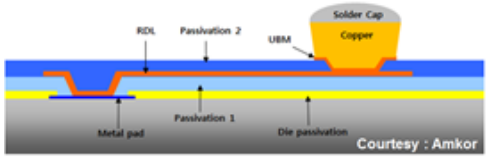


Figure 2-a. Typical structure of Cu bump with RDL

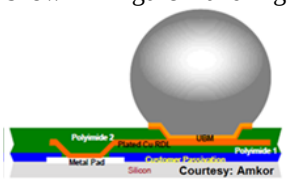


Figure 2-b. Typical structure of Solder bump with RDL

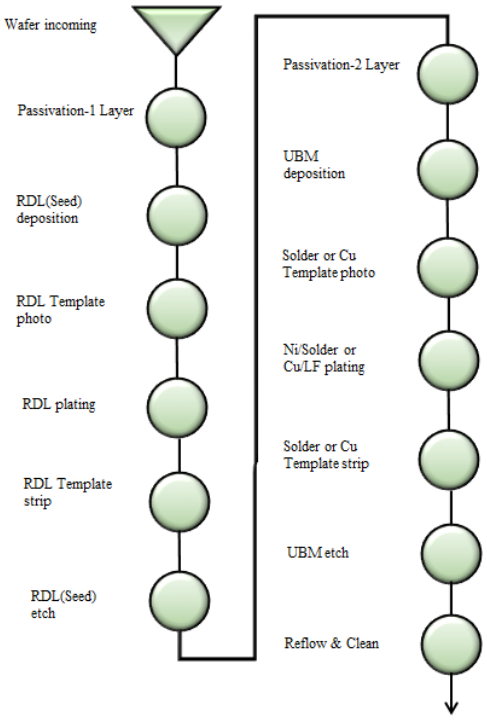


Figure 3-a. Process flow of RDL and Bump

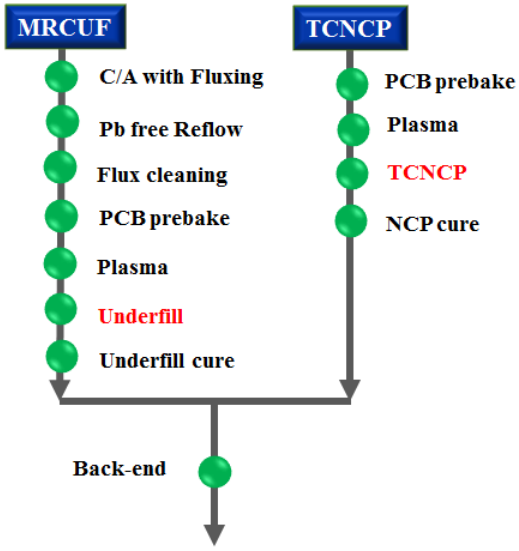


Figure 3-b. Process flow of Mass reflow CUF vs. TCNCP

3. Packaging Experimentation

3.1 Test Vehicles, Variables, and Boundary conditions

The objective of developing Fine Pitch Cu Pillar Technology is to establish a platform interconnection technology which can support a wide range of existing and future products. Hence, it is crucial to understand upfront the boundary conditions of each variable (i.e. bump pitch, die size, package type, substrate structure, etc.) and the reaction among factors. This is to ensure that the offering is an effective solution per the specific design and application. In conducting multiple experimentations in sequence, we have applied more extended design rules for the test vehicles than the baseline design rules (Table 1) already used for HVM (High Volume Manufacturing) production. This is to determine the technology extension capabilities.

Table 1. Baseline Design Rule in HVM

Package Body	Surface Finish	Die Size	BOT trace (Line/Space)	Bump Shape	Bump Pad Pitch
fcCSP	Electrolytic Sn plating (3-6um)	<10x10 mm^2 100um thick	20/20um	Ovular 20x45um UBM, 40um height	50um Inline
	Thin Ni/Au			Circular, 30um UBM, 40um height	40/80um staggered

- **Package body size**: 27x27mm^2 and 35x35mm^2 FCBGA with 1-2-1 build-up using 800um thick core (GX13/E679).
- **Package type**: Bare die, SPL (Single piece lid), and TCFCBGA (which is molded FCBGA, FCmBGA™).
- **Silicon die**: 1 metal layer daisy chain with 12x12mm^2 and 12x16mm^2, full stack 9 metal layer using 28nm node technology with 10x10mm^2 and 10x21mmm^2 (1x2 tiles of 10x10mm^2). The layout of the substrate top metal is shown in Figure 4. The full stack die test vehicle is to make sure we do not miss any critical reliability coverage from the 1 layer mechanical die TV.

- **Die thickness**: 500um and 780um have been evaluated to understand any impact from warpage.
- **Bump pad pitch**: Staggered 30/60um in two row and tri-tier staggered 40/80um for the Design For Manufacture study. The circular bumps are 30um in diameter with 40um height with a thicker SnAg solder cap, and Ovular bumps are 20x45um UBM with 40-45um height with a thinner SnAg cap (Figure 5).
- **Surface finish of package substrate**: Immersion Tin (IT), Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG).

Table 2. The factors and variables in the Test Vehicles

Package Body	Package Format	Surface Finish	Die Size	Die Thickness	Bump Shape	Bump Pad Pitch
27x27mm^2	Bare Die FCBGA	Immersion Tin	12x12 mm^2 (1 metal layer daisy chain)	780um	Ovular 20x45um UBM, 40~45um height	3 tier staggered 40/80 um (1 metal DC)
	SPL FCBGA	ENEPIG	12x16 mm^2 (1 metal layer daisy chain)			
35x35mm^2		DIG	10x10 mm^2 (28nm, 9 metal layer daisy chain)	500um	Circular, 30um UBM, 40um height	2 tier staggered 40/60um (28nm TV)
	FCmBGA	Solder Coat	10x21 mm^2 (28nm, 9 metal layer daisy chain)			
11x11mm^2 13x13mm^2	fcCSP (over-molded)	ENEPIG	<10x10 mm^2	100um	Circular, 23um UBM, 46um height	3 tier staggered 40/80 um

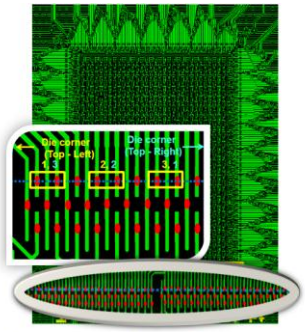


Figure 4-a. 12x16mm DC Substrate top metal layout

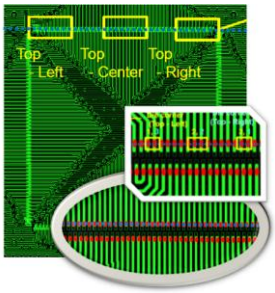


Figure 4-b. 10x10mm 28nm DC Substrate top metal layout

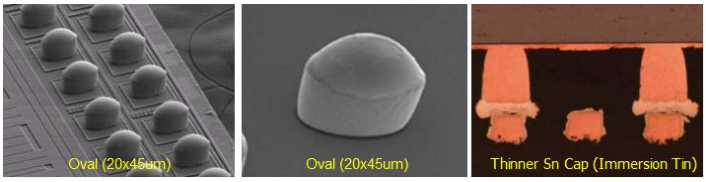


Figure 5-a. Ovular Bump and the BOT (Bond-on-Trace) on Immersion Sn

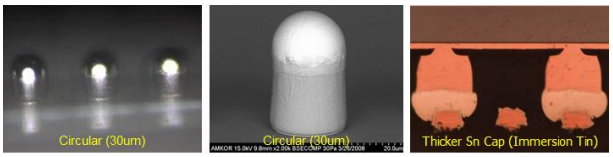


Figure 5-b. Circular bump and the BOT (Bond-on-Trace) on Immersion Sn

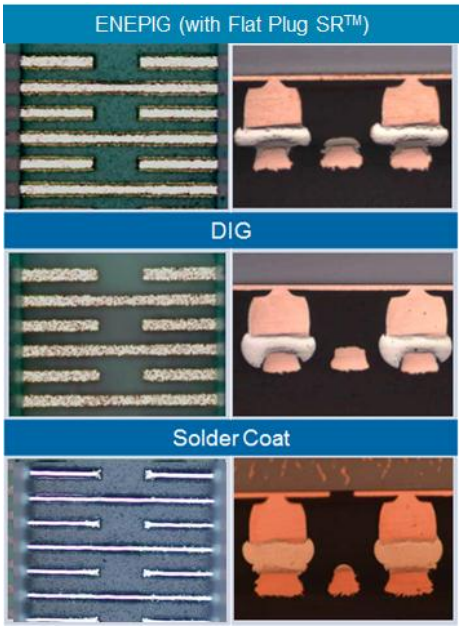


Figure 6. Other Surface Finishes and the cross-sections

3.2 Assembly

3.2.1 TCNCP

The TCNCP process for chip attach and underfill have been used for assembly due to the bump pitches being fine pitch. A typical TCNCP process is shown in Figure 7.

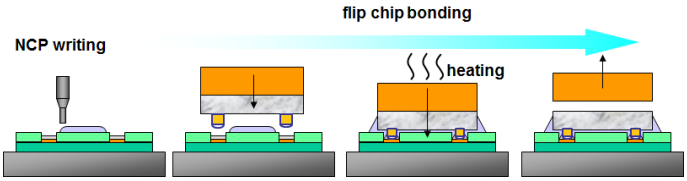


Figure 7. TCNCP process

TCNCP process characterization is very important for each and every new product due to the different combination of die size, die thickness and Cu pillar bump layout. This is essential to avoid reliability failures induced by improper manufacturing control. Good NCP(Non-Conductive Paste) coverage can be obtained by optimum NCP dispense pattern, volume, and bonding time and force. Visual inspection for checking the coverage and fillet height along die edge will be the first step. CSAM (Confocal Scanning Acoustic Microscopy) and/or X-ray is a non-destructive way for inspecting NCP voids, while p-lap (parallel lapping) is a destructive test method. Good alignment of the Cu pillar bonding on the substrate trace is another important item, which can be checked through x-ray inspection. Often, cross-sectioning at each corner of the dies is used for validating the off-set bonding. Lastly, checking solder wetting between the Cu pillar and substrate trace is the most critical step in the characterization. Cross-section is one of the methods for checking the solder wetting condition. Resistance measurement by electrical test prior to cross-sectioning would be the ideal way to locate any bonding has micro-cracking or discontinuity issues.

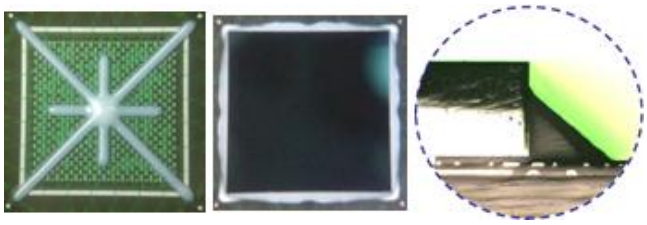


Figure 8. Example of NCP Dispense pattern, NCP coverage, NCP Fillet Height

3.2.1.1 Package Warpage and Coplanarity

Because the test vehicle packages are as large as 27mm and 35mm, it is important to understand the behavior of the package warpage and BGA coplanarity. Bare-die FCBGA package warpage and BGA coplanarity data show significant impact from body size and die thickness (Tables 3 and 4)

Table 3. BGA coplanarity per body size and die size/thickness

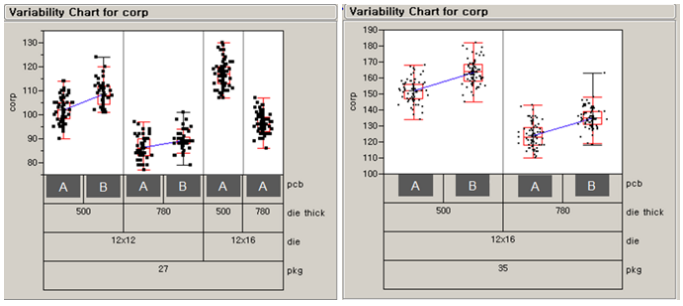
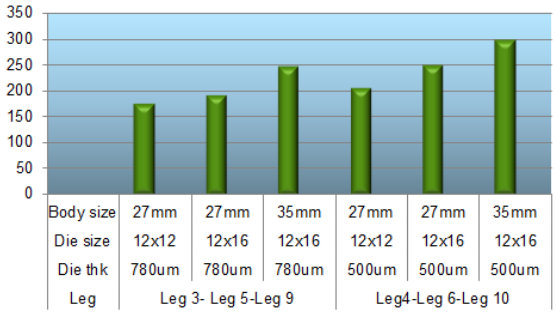


Table 4. Bare-die FCBGA Package Warpage trend



3.2.1.2 Reliability Tests

All test vehicles were subjected to the reliability stress tests per JEDEC Standards, as listed in Table 5. Besides, electrical Open/Short tests, SAM (Scanning Acoustic Microscopy) tests were performed for each readout point, time=0 and 200/500/1000/1500 hours/cycles.

Table 5 Reliability test items and conditions

Reliability Tests	Minimum Passing Limits
Moisture Sensitivity Level 3 (MSL 3) (30°C/60RH%)	192 Hours
Temperature Cycle "B" (-55°C / +125°C)	1000 Cycles
High Temperature Storage (150°C)	1000 Hours
Temperature Humidity Bias (THB) (85°C/85RH%)	1000 Hours
Unbiased HAST (130°C/85RH%)	96 Hours

4. Findings and Lessons Learned

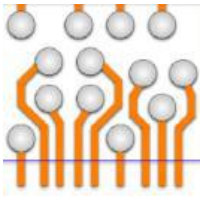
4.1 Substrate Design

4.1.1 Surface Finish

Electrolytic Sn or Ni/Au plating are common surface finish technologies that have been qualified and being applied for HVM BOT packaging. However, these technologies could be good for the packaging using strip format substrates with wider bump pitch (i.e. larger than 50um inline), but are not suitable for the single unit format packages with high density design (i.e. less than 50um bump pitch) due to tight DR (design rules) and cost. Alternatively, electro-less plating technology becomes a more cost effective solution for the devices requiring fine bump pitch TCNCP and BOT. Hence, we have evaluated Immersion Sn, ENEPIG (Electro-less Nickel Electro-less Palladium Immersion Gold), DIG (Direct Immersion Gold), and Solder Coat surface finishes as shown in Figures 5 and 6.

4.1.2 Substrate Structure

As it was already explained in Section-3 Design Enablement, there are many challenges on the design and layout of the substrate for TCNCP applications. Trench pattern solder resist opening is one of a common techniques which can accommodate larger number of IOs by utilizing limited space effectively. This pattern is shown in Figure 9.



Area Array Flip Chip Design

Fine Pitch Perimeter Flip Chip

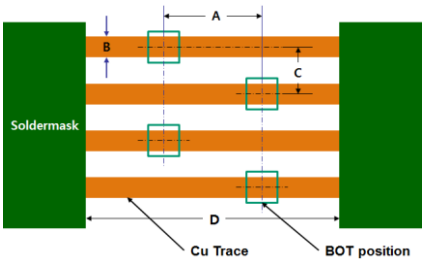


Figure 9. Trench Pattern Solder Resist Opening for BOT of fine pitch perimeter micro-bumps

4.2 Findings-1: Open failure from Immersion Sn plated test vehicle

Very obvious failures that we observed were open failures occurring at the interface between the Cu-pillar and BOT trace. The failure might be initiated from the Level-3 MRT (Moisture Resistance Test), and propagated further during temperature cycling (Figure 10). Most of failed pins are located on the middle row at the peripheral site. Larger body (35x35mm) and Thicker Die (780um) yielded higher open failures than smaller body (27x27mm) and thinner die (500um).

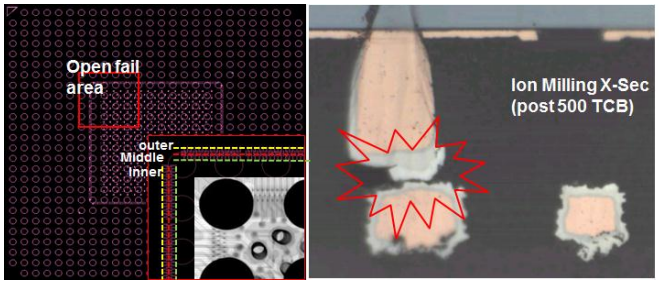


Figure 10. FA of open failure at 500 cycles TCB(Temperature Cycle, Condition 'B')

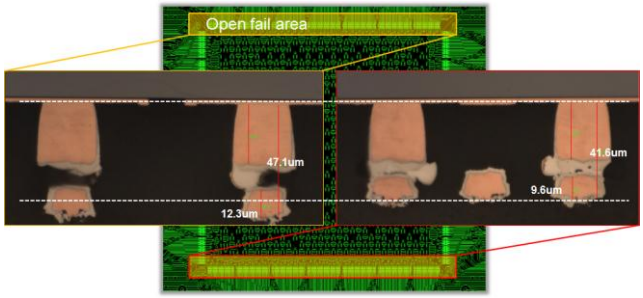


Figure 11. Commonality of location of opens failures

Figure 11 explains that die tilt might cause an insufficient solder joint at time zero and resulted in open failures after thermal cycling.

Figure 12 shows Cu undercut is prone to happen in the middle row of the trace, which might be proportioned to the plating time and/or length of Cu pad.

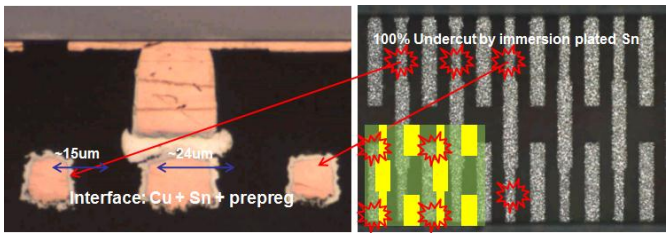


Figure 12. Cross section of Cu undercut

4.2.1 Lessons learned

Use of Immersion Sn as a surface finish for fine pitch device substrates has higher risks in micro-joint open failures due to Cu undercut and the insufficient amount of solder volume for the bump to trace joint. Major differences in Electrolytic Sn plating and Electroless Immersion Sn plating are the thickness control per the plating method. Electrolytic Sn plating is an additive plating, so the thickness can be added over 3um without impacting Cu, while electroless immersion Sn plating is a chemical substitution plating which replaces Cu. Therefore, thicker Sn plating thicknesses in Immersion Sn plating means there is more Cu undercut, which will result in more solder consumption in the micro-joint system, which end up yielding non-wetting (open failures) during thermal cycling.

4.3 Finding-2: Open failure from ENEPIG with Flat-Plug structure

4.3.1 Flat Plug structure

This is the structure where the SR (solder resist) is coated on the pad (trace) side-walls and plugs gaps between pads (traces). This technology is beneficial in helping to prevent Cu undercut, excess electroless plating, NCP trapped voids during the TCNCP process, and reinforcement of pad (trace) adhesion. The structure and advantages of Flat-Plug are shown in Figure 13-a and 13-b.

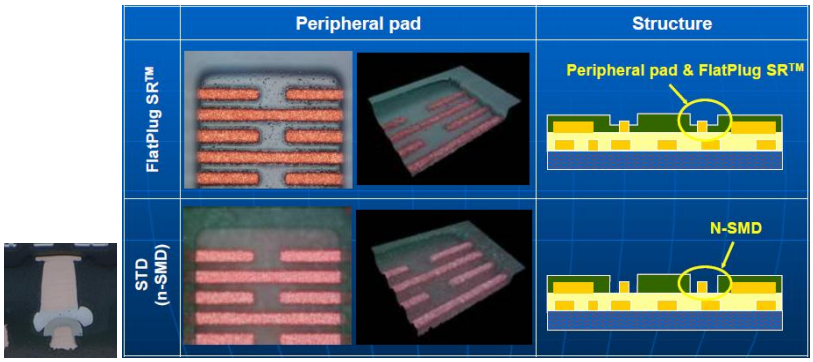


Figure 13-a. Cross-section and Structure of ENEPIG with Flat-Plug

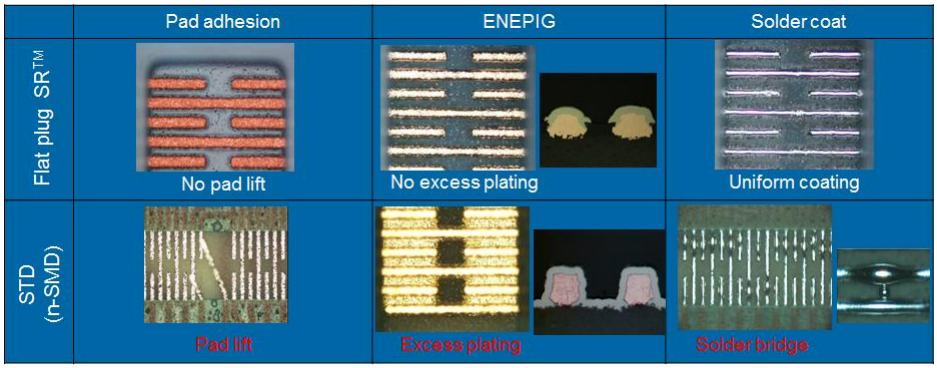


Figure 13-b. Advantages of Flat-Plug Structure

4.3.2 Mechanism of solder outflow on ENEPIG

Even with the use of the Flat-Plug structure with ENEPIG plating, we observed another obvious open failure during HTS (high temp storage). The open in the micro-joint happened due to the solder outflow over the ENEPIG surface, which results in insufficient solder. It was confirmed that the solder outflow is in proportion to the area of the ENEPIG bump landing pad. Figure 14 illustrates the mechanism of the open failure.

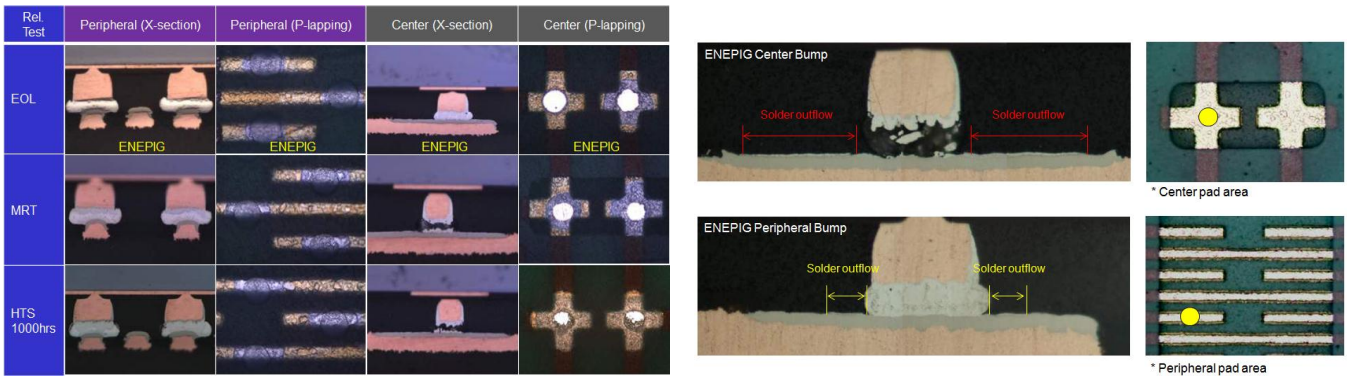


Figure 14-a: Progress of solder outflow during MRT (Moisture Resistance Test) and HTS (High Temperature Storage)
Figure 14-b: Solder outflow per landing pad area (ENEPIG)

4.3.3 Lessons learned

Changing the surface finish from Immersion Sn to ENEPIG for the Cu-bump bond on the trace was very effective. However, we have learned that the total area of the bump landing pad should be limited within some range because the excellent wettability of ENEPIG with solder will consume an extra amount of solder.

4.4 DIG and Solder Coat

Both DIG (Direct Immersion Gold) and solder coat surface finishes have demonstrated good wetting with SnAg solder of the Cu bump without Cu undercut. Though these two surface finish methods demonstrated good micro-joint interconnection and passed reliability tests, these options are yet to be favored for production due to the limited supply chain and being less cost competitive. The interconnection quality of post 500TCB (Temperature Cycle Condition 'B') is shown in Figure 15.

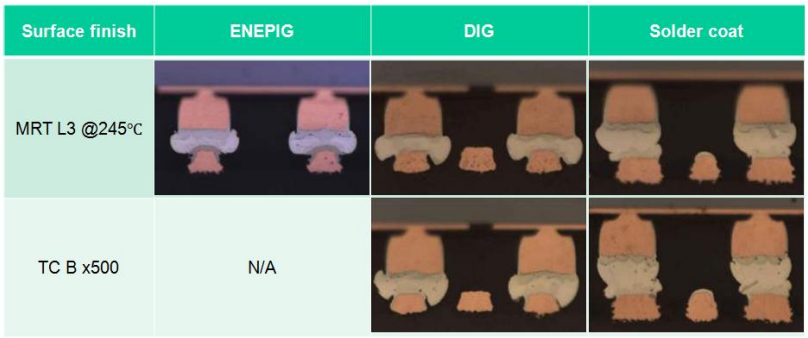


Figure 15. Cross-section of post 500TCB for DIG and Solder coat

4.5 Finding-3: ENEPIG on iSRO pad with Flat plug structure

Based on the lessons learned from multiple DOEs, it has been realized that the area of the bump landing pad for BOT will need to be kept as small as possible to minimize the solder outflow. Figure 16 is an innovative practice of structuring isolate solder resist opening (iSRO) with the Flat plug structure. The benefits of the iSRO with Flat Plug are not allowing Cu undercut but limiting the very small amount of solder outspreading. The structure of iSRO with Flat-plug is shown in Figure 16.

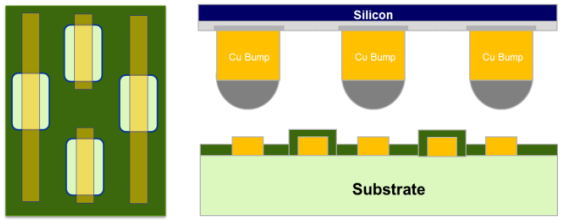


Figure 16. Design of iSRO BOT with Flat-plug

We have been able to demonstrate the robustness of the iSRO with Flat-plug structure in both TCNCP manufacturability as well as the long term CPI (Chip Package Interaction) reliability. The test vehicles used for the company technology qualification have passed 2000 cycles TCB (Temperature Cycle Condition 'B') and 1000 hours HTS and 96 hours uHAST (unbiased-HAST) with no failures so far. The actual cross-section of post 2000TCB (Temperature Cycle Condition 'B') is shown in Figure 17. Figure 18 shows the actual images of the Cu-bumps on chip and substrate top metal layers of the test vehicles evaluated.

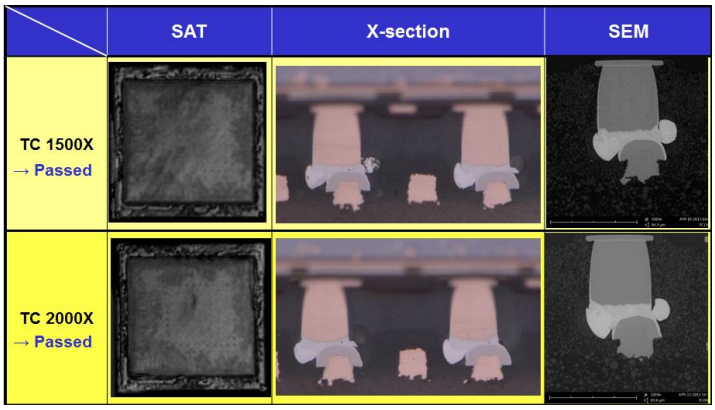


Figure 17. Cross-section of post 2000TCB bond of iSRO-Flat Plug

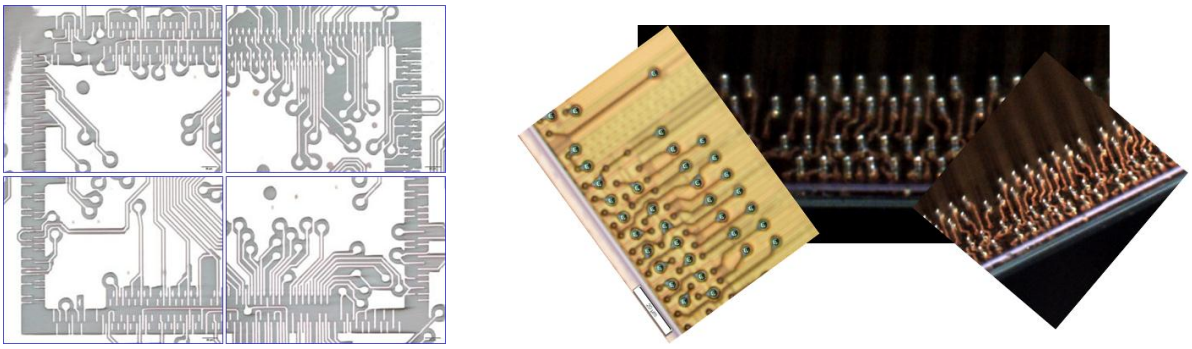


Figure 18. Actual substrate layer and Bump of the product SFF test vehicle

5. Conclusions

The comprehensive development work has successfully demonstrated the robustness of manufacturability and reliability of Cu-pillar micro-bumps and TCNCP using iSRO with Flat-plug structure substrates. A few additional engineering validations will be able to support even larger die (400mm^2) and larger body size FCBGA packages. All the learning from these series of experiments can help to identify a cost effective packaging solution where fine pitch Cu-pillar bump is necessary, too.

Finally, the technology has been applied for the successful launching of the company products. Additionally, this technology becomes a platform interconnection technology for cost effective advanced packaging (i.e. 2.1D and F2F), where high density micro-joint interconnection is required.

6. ACKNOWLEDGMENTS

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7. REFERENCES

[1] Yang-Gyoo Jung, Myung-June (MJ) Lee et al, “Development of Large Die Fine Pitch Flip Chip BGA Using TCNCP Technology” Electronic Components and Technology Conference, San Diego, CA, May 2012.

[2] JEDEC Solid State Technology Association. JESD22-A104D, Thermal Cycling.