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Device Miniaturization – The Impact of a High Density SoC Direct Chip Attach on Surface Mount and PCB Technologies

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Abstract
To keep up with shrinking system volume requirements for the Internet of Things and wearable devices while maintaining maximum device functionality requires an integrated approach to SoC and SiP optimization. To accomplish this we investigated the Direct Chip Attach (DCA) of a high density WLCSP onto the Printed Circuit Board (PCB) to obtain the smallest system footprint possible without compromising performance. Typically, to keep costs low, SoCs do not support the most aggressive interconnect density, and instead use wire-bond or large pitch flip chip packages to mount to the board. In this study, we take the opposite approach. Using DCA to attach the SoC directly to the PCB, we maximize the interconnect density between the board and silicon while keeping the cost low by eliminating the SoC package. This paper describes the impact of attaching a high performance SoC directly onto the board in terms of the PCB design, PCB fabrication and cost. We also investigate the SMT challenges of mounting the silicon directly onto the PCB at a 260 µm pitch array. Key metrics in this study include SMT yield, PCB routing, and PCB fabrication constraints as they relate to signal quality. In addition, the paper discusses future development challenges that face both the designers and PCB manufactures as they progress to support larger and denser direct chip attach products.

INTRODUCTION

Most SoC platforms utilize three unique interconnect routing topologies: silicon, substrate/packaging, and the PCB interconnect layers. All three work in harmony to allow I/Os as well as power rails to be redistributed to the various locations in the system. Each interconnect topology balances smaller/finer interconnects with the cost of manufacturing these finer features.

In certain applications the die/silicon interconnect density allows for a direct interface with the PCB, thus eliminating the package in the system. This application of DCA is commonly applied in many devices with Prismark predicting 30 billion DCA units shipping in 2014 [1]. What is unique about this DCA discussion is the large number of interconnects (N = 1675) at an array pitch that is as small as 260 um. This higher number of interconnects drove numerous tradeoffs in the PCB design, PCB manufacturing, and SMT assembly. The paper starts with the PCB design section which discusses the trade-offs in pitch, array pattern selection, and PCB stack-up topologies. It is followed by the PCB fabrication section which discusses the technology considerations that must be weighed to keep costs acceptable. In the final section the SMT results are shared to date with a discussion of the main variables such as paste types and underfill materials.

Point of clarification. DCA is used as the naming convention for a die singulated from a wafer which is then attached to a system board without first being assembled to a package substrate. This same “package” is also called WLCSP or WLP in the industry.

PCB Design

Designing for higher density DCA footprints require manipulating combinations of several key design features in order to achieve an adequate pad size for a reliable solder joint. There are direct relationships between the rules and changing one will have a rippling impact on the others. Therefore staring with the DCA pad array one can work inward to understand microvia dimensions, dielectric thicknesses to develop a first order stack-up. Figure 1 outlines a few common design features required for constructing a BGA/DCA footprint. For instance, the outer layer microvia pad diameter and BGA/DCA solder pad diameter design requirements will align to the larger of the two pad size rules. Microvia-to-pad registration tolerance drives the microvia pad size on the internal layer (labeled “bottom” on the figure). The microvia dielectric thickness drives microvia diameters, and as pitch decreases, the opposite begins to happen – microvia diameters drive the dielectric thickness, which then impacts impedance targets and tolerances. Solder mask registration and pad size openings often help determine the external layer pad-to-trace spacing design rule. All these tradeoff combinations were iteratively addressed and specific values sets are discussed in later sections of the paper.

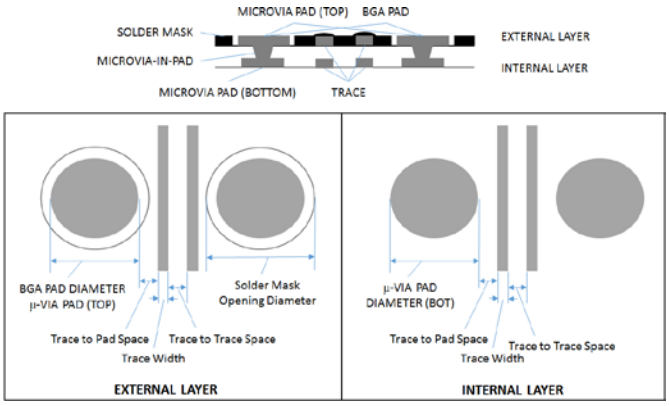

Figure 1: Standard Board and Package Design Rule Descriptions

Once an acceptable set of variables is defined for the DCA array, rules for optimizing trace width and trace-to-feature spacing are important to review with manufacturers. Most board fabricators will prefer line width reduction before spacing reduction because in a subtractive process, the manufacturer actually fabricates spaces and not traces. Along the same lines, adequate spacing is necessary around controlled impedance traces to allow for trace width compensation. To layout the various DCA test boards, we worked closely with four of the top 10 volume suppliers [2] experienced with high density designs to discuss many of these fabrication rule trade-offs. It became apparent that in order to achieve lowest total platform cost the PCB design rules needed to remain at the limits of the modified semi-additive process (mSAP). In other words, we preferred to stay with the subtractive process, albeit pushing to the leading edge manufacturing limits of the process. Now that the DCA pad rules were forming and the PCB trace and spacing rules were forming, we moved on to the DCA array pattern selection that allowed for maximum routing density for the given rules.

Board designer BGA/DCA routing breakout concepts and schemes have significant impacts on the aforementioned design rules. Design patterns (aka footprints or schemes) may be utilized that do not require routing at minimum pitch on external layers, therefore minimizing the impacts of trace-to-pad design rules. In addition, the number of traces routed between microvia pads may change as a function of targeted routing density and layer counts used.

I/O density goals and design schemes guide routing constraints and establish design rule targets. Figure 2 illustrates different land pattern schemes. The square land pattern [A] simple in design is difficult to optimize as the minimum pitch is applied in both the horizontal and vertical direction. The presence of a trace between lands would require aggressive design rules and fabrication capabilities. An alternative, the rectangle pattern [B] allows a larger pitch between lands when a trace is present. This pattern requires some corner optimization. However, with a rectangle pattern only one axis is at minimum pitch. The face-centered-rectangle pattern (FCR) [C] provides optimal packing density as edge and diagonal pitch are defined by design rule minimums driven by PCB fabrication capabilities.

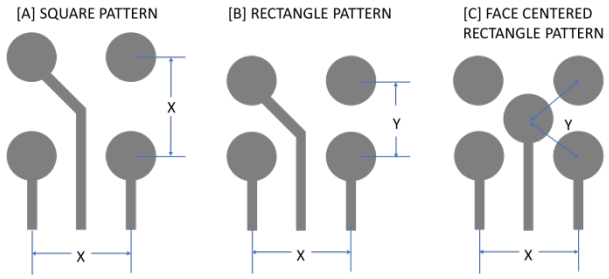

Figure 2: DCA/PCB Land Pattern Schemes

Design tools and processes have improved to enable complex board designs. Traditionally board level routing has been conducted at angles of 45 degrees and in support of orthogonal connections. The FCR pattern coupled with minimum pitches necessitates odd angle routing and centered routing [3]. Odd angle and centered routing is needed to evenly provide design balance for the manufacture of the printed circuit boards. Unbalanced routing between the die bumps unnecessarily increases the risk for shorts between different nets.

The board may require redistribution of interconnectivity across adjacent layers. The board scheme should be devised to balance manufacture risk while maintaining good signal integrity practices, crosstalk, return path and power delivery considerations. It is standard practice to route signals on alternating layers (signal-ground-signal, etc.) providing adjacent return paths [4]. However,

as signal counts increase and silicon redistribution restricted increasing local density on the DCA designs, an alternate method was required to route signals. Signal lines are fanned out on both the routing layer as well as the reference layer. Once there is sufficient space, routing is merged back into one routing layer and the reference plane is reintroduced. To minimize crosstalk, cross-over routing is offset between layers. Figure 3 shows an example of board level routing on adjacent layers. A composite view demonstrates offset routing between one layer (blue) and the adjacent layer routing (red) to minimize crosstalk. Stitching ground vias in the front and back of the signals were used to improve the return path. The design allows for one signal track to escape at a larger edge pitch along with outer row signals for the specific layer. This design practice was used with the functional DCA test board. To date, we have not fully analyzed the signal quality impact of utilizing the cross-over routing. Modeling suggests it is an acceptable impact for our given product.

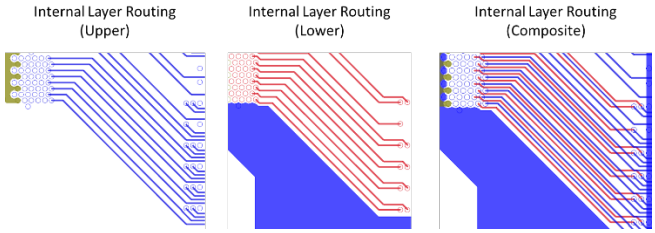

Figure 3: Board Routing Redistribution Example.

The final design attribute to discuss is the microvia rules. Considering a single track routing approach, the microvia and its associated capture pad drive the final array pattern's density. In the example of a DCA breakout shown in Figure 4, the single track pitch of 320 um allows for 50 um trace width and 50 um trace to pad spacing. Key points to this example are the alignment of the pad diameters and microvia-in-pad design rules. The pad size functions as the interconnect to the DCA. The size is important to ensuring a robust connection in addition to manufacturability and test capability. The microvia pad size sets the basis for determining the microvia diameter, which then may influence dielectric thicknesses. As the microvia pad decreases in size, the microvia diameter will follow otherwise risking microvia breakout issues.

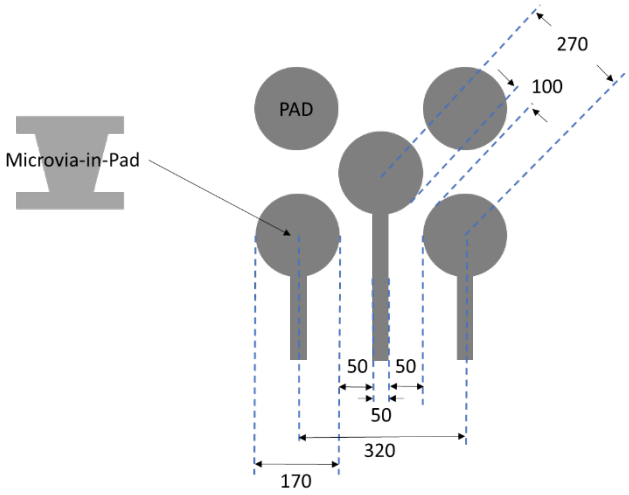

Figure 4: Surface Design Rules Applied to Breakout. (units in microns)

PCB FABRICATION

PCB layout design rules were carefully selected to pair with high volume manufacturing (HVM) PCB fabrication capabilities since PCB fabrication limitations can yield an unreasonable and costly design. In this paper we covered three DCA test boards using existing subtractive board technology to a minimum pitch of 210 um. Board designs below this pitch were found to be prohibitively complex and expensive. Since most Si manufacturers can produce and test die with pitches at 150 um and below, this implies that DCA products are required to fan-out to larger pitches or to select a subset of signals that won't require the full pin count at the minimum pitch. Higher complexity SoCs need to be studied to best understand their fit as a DCA product.

Since every PCB manufacturer has their own processing recipes and yield expectations, no single design rule values could be aggregated for feature dimensions. However it was apparent that around 30 to 40 um, a processing change occurs. Figure 5 provides a reflection of design rules as a function of board manufacture technology considerations. Best estimates suggest the overall PCB bare board cost would increase by 50% if we designed trace and space below 30-40 um.

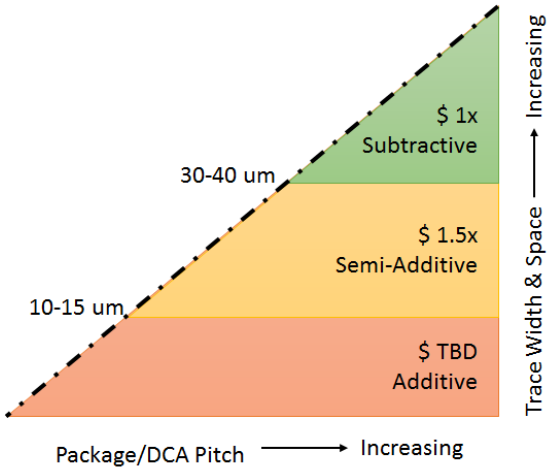

Figure 5: Board Manufacturing Technology Considerations

Beyond the PCB manufacturing of routing features, one must also find an acceptable microvia pad stack. Larger microvia diameters in small pads may break-out resulting in high defect rates and compromised reliability. Preferred microvia to pad registration is roughly +/- 60 um for a typical cell phone board built today. However, advanced designs are pushing +/- 37 um or even less. Thus a preferred pad size for a 100 um microvia is roughly 220 um, but tighter densities are pushing, for example, a 75 um microvia in 150 um pads. The manufacturer is faced with the challenge of reducing microvia diameters, maintaining optimal aspect ratios for drilling (thinner dielectric), while still having to meet impedance requirements. A 60 um dielectric thickness is fairly common today with designs pushing 50 um and less. This in turn will drive 50 um or thinner traces to maintain the same impedance.

Design rules and tolerances are generally different between the various features as well. For example, solder mask processing typically requires additional fabrication allowances versus copper processing. The fabricator can often hold better tolerances of etched features than solder mask features, not to mention solder mask also requires a registration tolerance of +/- 37 um or more depending on the exposure equipment used. In such a case, the spacing between metal defined pads increases to accommodate solder mask dams versus solder mask defined pads as shown in Figure 6.

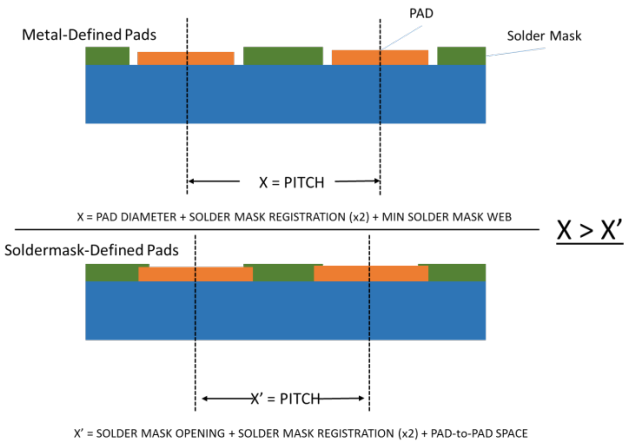

Figure 6: Pad Definition Type Impact on Minimum Pitch

Of course, the final DCA footprint will determine if metal defined pads or solder mask defined pads can be used. Another option is to eliminate solder mask in the DCA region altogether, thus removing one design and fabrication barrier to producing tighter densities required for higher I/O count DCAs. We performed a small experiment where we varied the solder mask opening from 125 um diameter (SMD125) , 150 um diameter (SMD150) and completely removing the solder mask in the DCA pad array (NSMD no mask). Figure 7 plots solder volume paste inspection results for the three treatments. The plot indicates a large number of insufficient paste pads on the array without a solder mask. The leading theory is the insufficient prints may be attributed to the open area around the pads with no support to the stencil during printing. A smaller aperture is the next step in investigating the opportunity [5].

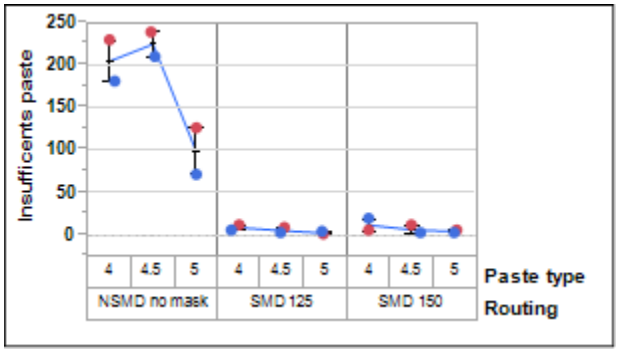

Figure 7: Pad Definition Type Impact on Minimum Pitch

To summarize our specific findings, we provide Table 1 below with key PCB parameters used during the DCA studies. The 210 um pitch functional test board drove leading edge subtractive processing of which solder mask was an area of difficulty.

Table 1: Test Board Features

	Test Board		
	A	B	C
Board Type	SMT test design Limited routing (daisy-chain configuration)	JEDEC test board Limited routing (daisy-chain configuration)	Functional product with full routing
Board Construction	2-6-2+ Mid-Tg HF	2-6-2+ Mid-Tg HF	10 layer any-layer Mid-Tg HF
Board Thickness (mm)	0.65	0.65	0.8
Minimum DCA Pitch (um)	300 side 1 260 side 2	260	210
DCA Quantity	6 side 1 4 side 2	15 side 1 15 side 2	1
Die Size (mm)	7.5x7.5 side 1 10x10/6x6 side 2	10x10 side 1 6x6 side 2	10x10
Pin Count	676 side 1 1675/603 side 2	1675 side 1 603 side 2	2349 (excludes depop)
Min. Outer Layer Trace/Space (um)	N/A Jumpers only	N/A Jumpers only	50/50 breakout 60/60 routing
Min. Inner Layer Trace/Space (um)	N/A Jumpers only	N/A Jumpers only	50/60
DCA Pad Diameter (um)	230 side 1 210 side 2	210	160
DCA Pad-Pad Spacing (um)	70 side 1 50 side 2	50	50
Microvia Diameter (um)	75	75	75
Microvia IL Pad Diameter (um)	175	150	150
Solder Mask Opening (um)	170 side 1 150/125 side 2	150/125 side 1 150/125 side 2	160 (1:1 w/ pads)
Solder Mask Registration (+/- um)	30 side 1 30/42.5 side 2	30/42.5 side 1 30/42.5 side 2	Best Efforts
Surface Finish	ENiG/OSP	ENiG/OSP	ENiG

In order to drive for finer component pitches, developing supporting technologies is required. Subtractive processing alone will not suffice. It will be necessary to invest in semi-additive fabrication technology and eventually fully additive processing. This could be approached as a paradigm shift by not designing and fabricating each interconnect level separately, but rather as a sum of the whole. As alluded to in the previous section, the silicon designer must take into account board design and fabrication schemes and rules. Assembly processes may need to compensate for PCB fabrication limitations. For example, eliminate the use of solder mask when designing DCAs under a specific pitch. This means pads only on the outer layers, but the tradeoff could potentially result in reliability issues since no insulating material now exists between the tightly spaced pads. Assembly materials could potentially compensate for this, such as using an underfill that achieves the necessary mechanical constraints while also substituting as the missing solder mask. Table 2 depicts a generalized technology breakdown versus pitch reduction

comparing the square DCA footprint (aka scheme) with a HEX pattern. Several assumptions were made just to illustrate the evolution between design scheme, PCB technology, and board features as the pitch is reduced.

Table 2: Technology Versus Pitch Reduction

	*DESIGN ASSUMPTIONS (um)		
PITCH (mm)	SQUARE SCHEME 4-sided routing	**HEX SCHEME 2-sided routing	TECHNOLOGY (generalization only)
0.40	325 OL pad / 250 SRO +/- 37.5 SM reg 100uvia/220pad IL 1 track IL routing 60/60/60 sp/tr/sp	325 OL pad / 250 SRO +/- 37.5 SM reg 100uvia/220pad IL 1 track IL routing 150/150/150 sp/tr/sp	Subtractive processing; Std photo-imaging; May use SM LDI
0.35	275 OL pad / 215 SRO +/- 30 SM reg 75uvia/180pad IL 1 track IL routing 60/50/60 sp/tr/sp	275 OL pad / 215 SRO +/- 30 SM reg 100uvia/220pad IL 1 track IL routing 125/125/125 sp/tr/sp	**SQ:** Subtractive processing; LDI including solder mask **HEX** Subtractive processing; Std photo-imaging; SM LDI
0.30	225 OL pad / 175 SRO +/- 25 SM reg 75uvia/150pad IL 1 track IL routing 50/50/50 sp/tr/sp	225 OL pad / 175 SRO +/- 25 SM reg 80uvia/200pad IL 1 track IL routing 100/100/100 sp/tr/sp	**SQ:** Subtractive processing; LDI; special (S&R?) SM LDI **HEX** Subtractive processing; std photo-imaging; special (S&R?) SM LDII
0.25	190 OL pad / 150 SRO +/- 20 SM reg 60uvia/130pad IL 1 track IL routing 40/40/40 sp/tr/sp	190 OL pad / 150 SRO +/- 20 SM reg 75uvia/175pad IL 1 track IL routing 85/85/85 sp/tr/sp	**SQ:** Subtractive/**mSAP** transition LDI; **uvia devlp;** SM not feasible **HEX** Subtractive processing; std photo-imaging; SM not feasible
0.20	150 OL pad / 120 SRO +/- 15 SM reg 50uvia/100pad IL 1 track IL routing 30/30/30 sp/tr/sp	150 OL pad / 120 SRO +/- 15 SM reg 75uvia/150pad IL 1 track IL routing 65/65/65 sp/tr/sp	**SQ**: **mSAP processing;** **uvia devlp** **HEX:** Subtractive; std photo-imaging; SM not feasible
0.15	110 OL pad / 90 SRO +/- 10 SM reg 45uvia/90pad IL 1 track IL routing 20/20/20 sp/tr/sp	110 OL pad / 90 SRO +/- 10 SM reg 50uvia/100pad IL 1 track IL routing 50/50/50 sp/tr/sp	**SQ**: **mSAP; uvia devlp;** SM not feasible **HEX:** Subtractive; **uvia devlp**; LDI; SM not feasible
0.10	80 OL pad / 70 SRO +/- 5 SM reg 35uvia/70pad IL 1 track IL routing 10/10/10 sp/tr/sp	80 OL pad / 70 SRO +/- 5 SM reg 35uvia/70pad IL 1 track IL routing 35/30/35 sp/tr/sp	**SQ**: **Need radical devlp** **HEX: mSAP** transition; **uvia devlp**; LDI; SM not feasible

* Reference only; it is understood the design can vary depending on supply base capability
Typically breakout routing only. Assume solder mask defined pads (SMDP)
** 1-track routing for comparison only; HEX pattern capable of denser breakout routing

History has shown that transitioning to a new technology, such as semi-additive fabrication, will likely cost more initially driven by new processes and equipment, lower production yields, and market pricing. However, as more companies move the same direction, improvements in high volume manufacturing and competition will drive prices down. For example, Figure 8 depicts microvia board pricing as a function of time as experienced with actual HVM product over time.

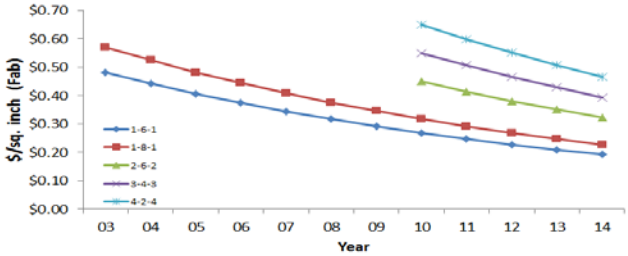

Figure 8: HDI Cost Trend

As the PCB industry transitions to a fully additive technology, one would expect to see the same curve with higher prices initially and a slow decline over time. A fully additive fabrication process means less waste, fewer process steps, and likely higher yields. Figure 9 compares the semi-additive process with a fully additive technology. There remain significant process challenges to be addressed for a fully additive process. First is the operating costs to maintain cleanroom standards. Second is processing speeds such as the high speed electroless chemistry, microvia copper filling for stacking microvias and plating of through holes (buried vias), the prospect for high density additive process PCBs is promising.

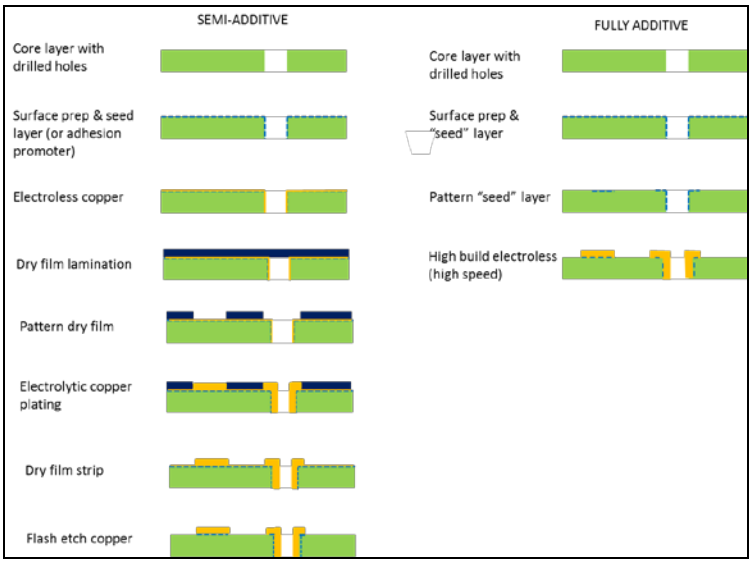

Figure 9: Semi-additive Versus Fully Additive Process Steps

SMT CHALLENGES

Since it requires reducing the stencil aperture dimensions, stencil printing of fine pitch DCA is a challenge. In order to keep an adequate area ratio the stencil thickness needs to be reduced, and in order to form a reliable joint, a Type 5 paste may be needed. Solder paste transfer efficiency, defined as the printed solder paste volume from the stencil divided by the expected theoretical calculated volume, is a well-known indicator of the printing process [6]. Figure 10 shows transfer efficiency of a 140 um (5.5 mil) round aperture using a 50 um (2 mil) thick laser cut stencil with nano-coating to help increase the paste transfer as calculated for two pastes from different sources.

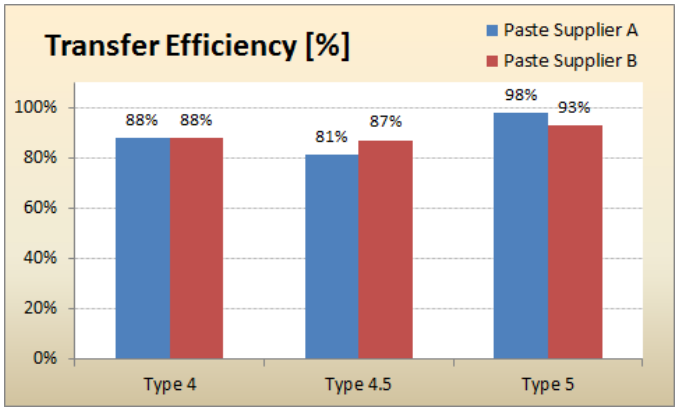

Figure 10: Solder Paste Transfer Efficiency

The experiment shows, for both suppliers, an improvement in printing transfer efficiency when decreasing the powder size from Type 4 to Type 5. Type 4.5 did not show any improvement in paste transfer rate.

Once the stencil printing process was deemed acceptable, the next step was to show SMT assembly proof of concept. Several DCA packages were assembled using two different test vehicle boards (Table 1, boards A and B). An example of a JEDEC test vehicle board is shown in Figure 11. SMT yields were assessed using a board-to-die level daisy chain pattern to identify open solder joints and X-ray to identify bridging. The SMT feasibility study was done on a total of 400 DCA packages with an overall yield of 87.2%. Figure 12 shows the SMT yield versus assembly variables. The 780 um thick die had low yields related to incoming material quality such as missing and damaged micro-balls. These results indicated the SMT assembly process was feasible. Test board C is under evaluation as of the writing of this paper and therefore was not included with the SMT test results.

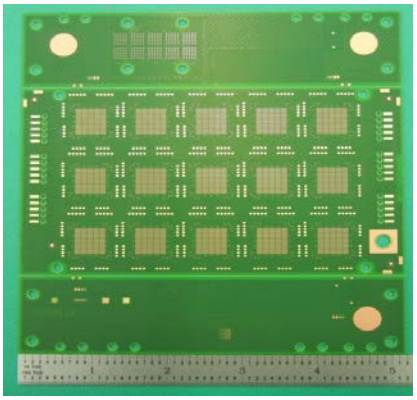

Figure 11: JEDEC Test Board

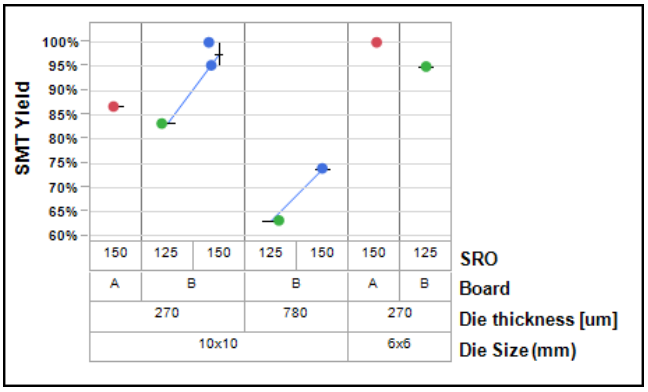

Figure 12: SMT Yields

Mechanical shock (drop) and thermal cycle testing were completed on separate JEDEC test boards. The standard JEDEC-B111 drop test at 1500G was performed on six boards with and without board level underfill (BLUF). Boards were fully populated with 15 10x10 mm die (larger die = worse case).

Results clearly indicated BLUF was necessary to pass the drop test (minimum 30 drops) – as shown in Table 3. It must be noted this test was performed on a small sample size as a feasibility study only. However, results do support the fact that BLUF is recommended to ensure adequate DCA-to-PCB solder joint reliability under mechanical stress conditions.

Table 3: Drop Test Results

# Boards	BLUF	# Drops	Pass/Fail
4	NO	All < 30	Fail
2	YES	Both > 100	Pass

Thermal cycle profile testing was performed from -40 C to 100 C with a 60 minute cycle using two JEDEC test boards with four 10x10 mm die each. Die with and without wafer level underfill (WLUF) were used. Results (Table 4) indicated WLUF performed better at twice the number of thermal cycles than no WLUF, but it must be emphasized this was also only a feasibility test with a small sample size. It must also be noted that neither passed thermal cycling requirements. Extensive cross-sectioning showed voiding at the first level interconnect layer which likely resulted in premature failures – see Figure 13.

Table 4: Thermal Cycle Test Results

Test Board	# Thermal Cycles	# Daisy Chains	# Daisy Chain Failures	WLUF
1	100	16	13	NO
2	200	16	9	YES

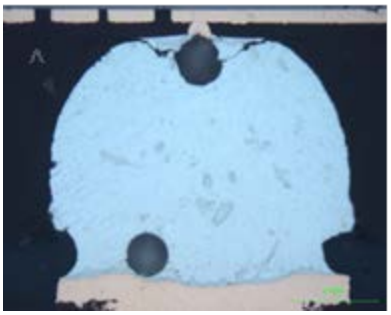

Figure 13: First Level Interconnect Voiding

SUMMARY

Direct Chip Attach of high density and high signal count SoC devices provides a clear advantage in both size and functionality for wearable and Internet of Things products. We have provided our view of the PCB design rules required to scale into the 150 um pitch range. We provided examples of manufactured PCBs that were at the limits of subtractive processing and scaled to support a 210 um pitch DCA product. We discussed the value of mSAP and fully additive PCB manufacturing and how these process changes could be beneficial for smaller and arguably low cost PCBs. We provided some SMT data we have collected to date to defend the design choices and discuss trade-offs between SMT assembly and PCB manufacturing (ex. soldermask). While there are several technology barriers and initial costs, we foresee the value to grow the DCA capability to include products as complex as SoCs.

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